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Sumitomo Electric Industries and others start transmission tests in real grid, Albany, USA, using high-temperature superconducting (HTS) cable

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Electric Power and Energy Research Laboratories
Sumitomo Electric Industries, Ltd.

A grid connection test of a high-temperature superconducting cable was started on July 20, 2006 under the High-temperature Superconducting Cable Project (Albany Project) of the United States funded by the Department of Energy (DOE) and New York State Energy Research & Development Authority (NYSERDA). Participating in the project are Sumitomo Electric Industries and other companies. The high-temperature superconducting cable is a bismuth-based high-temperature superconducting cable of 350 m in length and is installed in the world's first live long-length underground power transmission line along which a conduit with an inside diameter of 150 mm. The verification test of the superconducting cable system will be conducted for about six months. SuperPower, BOC and National Grid are participating in the project with Sumitomo Electric Industries. On August 2, a gala event commemorating the completion of the facility was held attended by about 200 persons including Governor Pataki of New York State and other invited guests. President Matsumoto of Sumitomo Electric Industries also attended the event. More than one month after starting power transmission, power is stably supplied and the superconducting cable is transmitting power unattended by operators.

Fig.1 Installation map of high-temperature superconducting cable

The Albany Project is a verification test project of a superconducting cable system undertaken in Albany, the capital of New York State and a hub in the power grid of New York State. A 350-m superconducting cable was installed between two substations of National Grid at Riverside and Menands at a distance of about 3 km for verification tests by connecting a superconducting cable to a real transmission line. The high-temperature superconducting cable manufactured by Sumitomo Electric Industries is a superconducting cable of a three-in-one type with three cable cores jacketed together in a one thermal-insulated pipe. The cable construction withstands shrinkage during cooling and heat cycles between room temperature and liquid nitrogen temperature and is compact. Transported by a ship from Kobe Port to America, the superconducting cable was installed using the same installation method as that for conventional power cables. The superconducting characteristics and characteristics of the thermal-insulated pipe have not changed after transport and installation, evidencing stable characteristics. The 350-m cable was split into 320-m and 30-m sections, and the sections are joined by a cable joint for the first time in the world, paving the way for the installation of more superconducting cables in power

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transmission and distribution lines in the future. The terminals at both ends of the cable and cable joint are of a three-in-one type with three cable cores in one vessel. In March 2004, Sumitomo Electric Industries commissioned a commercial-volume production process for bismuth-based high-temperature superconducting wires using a high pressure sintering method, i.e. Controlled Over Pressure method. The superconducting cable installed in Albany uses 70 km of bismuth-based high-temperature superconducting wires manufactured by the this method featuring excellent mechanical and electrical characteristics.

In the United States, the Energy Act enforced in August 2005 regards modernization of the grid by high-temperature superconducting cables as a national task, and a program to build a sturdy superconducting cable grid throughout America by 2030 is being studied (Grid2030). As part of this program, superconducting cable projects funded by DOE are also being undertaken in Columbus, Ohio, and Long Island, New York. The construction of the Albany Project was completed first among these projects, and a verification operation on a live power transmission line was started. One great step has been taken toward the commercial production of high-temperature superconducting cables in the future.

Fig. 2 Three-in-One type high-temperature superconducting cable with three cable cores jacketed together

Fig. 3 Three-in-One Joint of three-in-one type high-temperature superconducting cable

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Mechanism of High-Temperature Superconductivity "Phonon Rekindling"

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In high-temperature superconductors also, superconductivity is triggered by the formation of electron pairs (Cooper pairs). The starting point of the BCS theory in low-temperature superconductors is that the attractive force of electron pair formation is mediated by phonons. It is well known that an experimental basis for this is variation of T_c by isotopic substitution. Since then, both experiments and theories have been made precise, and T_c is now forecasted from data on measurement of the coupling strength of electrons and phonons from the characteristic (dI/dV, d^2I/dV^2) of current I flowing across a superconducting tunnel junction to voltage V.

Similar techniques have also been used with high-temperature superconductors. However, the majority view has been that phonons are not involved in high-temperature superconductivity because of a small isotope effect and because significant data could not be obtained from tunneling spectroscopy. On the other hand, various spectroscopies have been advanced thanks to high-temperature superconductivity research, enabling collection of information on electrons and phonons in much more detail than before. One typical example is photoelectron emission spectroscopy and scanning tunneling microscopy (STM). Beginning this century, advances in these two techniques have contributed to making phonons visible also in high-temperature superconductors. [1),2)]

A recent STM experiment examined tunnel current characteristics on an atom scale. [2)] Resolution of the atom scale is needed because the size (Δ) of superconducting gap varies in accordance with the nanometer scale and because a normal tunnel junction method spatially averages important information and hides it. As in Δ, the characteristic features measured with Bi-based high-temperature superconductors vary on a nanometer scale. Clear structures were observed in spectra in various places. In the case of low-temperature superconductors, this structure corresponds to phonons that mediate the attractive force between electrons. Isotopic substitution of oxygen atoms was performed to analyze the origin of this peak, and its energy position moved. When the mass of oxygen atoms varied with isotope substitution, the phonon

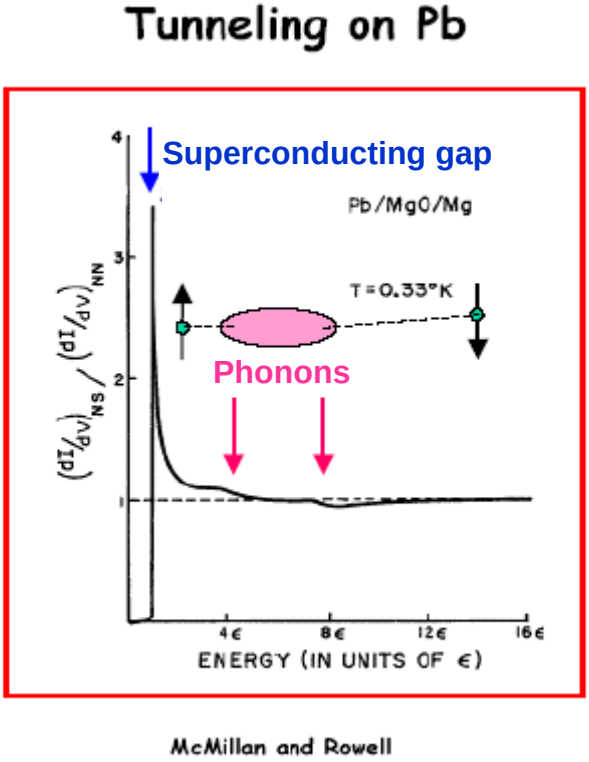

Fig. 1 Phonons involved in Cooper pair formation are visible in low-temperature superconductors judging from the characteristics of tunnel junction.

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frequency (Ω) varied correspondingly. Undoubtedly, phonons were "visible."

This result does not assert that phonons are acting as an adhesive in Cooper pair formation of high-temperature superconductors. For example, Ω varies in isotopic substitution, whereas *Δ* hardly varies. (T_c does not vary, either) However, it is certain that phonons play some role in the emergence of high-temperature superconductivity. How to think of phonons has become a hot topic in the research of high-temperature superconductivity coupled with spins and charges of electrons.

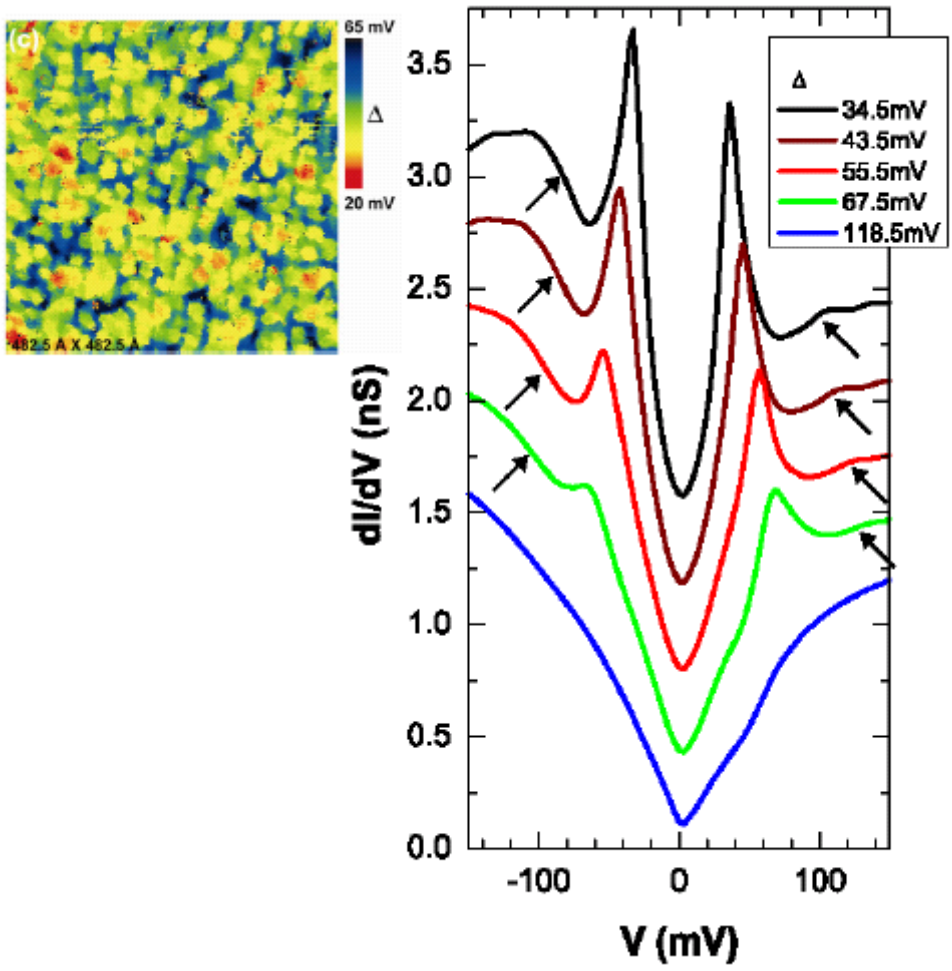

Fig. 2 An STM probe is needed to view "phonons" (arrow) because a superconducting gap spatially varies on a nanometer scale.

References:

1) A. Lanzara *et al.*, Nature **412** (2001) 510-514.
2) J. Lee *et al.*, Nature **442** (2006) 546-550.

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Report on the 15th International Superconductivity Industry Summit

The 15th International Superconductivity Industry Summit was held in Erlangen, Germany on Thursday, September 28, and Friday, September 29, 2006. Participating in the Summit meetings were about 40 representatives from Japan, the United States, Europe, Korea and China. The city of Erlangen is also known for the Erlangen program in which mathematician Klein showed an approach for the foundation of modern geometry prior to assuming professorship of Erlangen University that "Geometry is to examine invariable quantities under a transformation group characteristic to the specific geometric system."

The theme for the summit meeting this year was "20 Years of High-temperature Superconductors - Successes and Challenges." Representing Japan, four lecturers including Prof. Tanaka, Vice President of ISTEC, reported the current status and future of high-temperature superconductors in Japan. Development competition between Japan and the United States is intensifying on next-generation wires. In the United States, verification programs for superconducting cables are now underway in Columbus, Ohio, Albany, New York, and Long Island, New York, under the Superconductivity Partnership Initiative (SPI) funded by the Department of Energy (DOE). Energizing tests have been started with the first two of the three projects and Sumitomo Electric Industries of Japan is also participating in the Albany Project. In Europe, efforts are being made to use high-temperature superconductors in motors. Representatives from Korea and China participated in the summit meeting this year. In Korea, the Center for Applied Superconductivity Technology (CAST) was established under the Ministry of Science and Technology, undertaking research and development of superconductivity in wide-ranging fields from electric power to electronics between 2001 and 2010 (2001 to 2003 for Phase 1, 2004 to 2006 for Phase 2 and 2007 to 2010 for Phase 3). In China, superconductivity is regarded as one of important technologies included in the National Medium- and Long-range Science and Technology Development Plan. The superconductivity projects of China focus on development in various fields of superconducting wires including cables, FCLs and filters. China is undertaking the Yunnan and Lanzhou Projects on superconducting cables in a bid to catch up with Japan, the United States and Europe.

Steady progress has been made in the commercialization of superconductivity in the fields of high energy including nuclear fusion, experiment apparatus and medicine. Nevertheless, it is generally felt that further endeavor is needed for further commercialization. Steady high-temperature superconductivity development efforts in particular has great importance for the future promise early commercialization. As mentioned above, the development of superconductivity is being accelerated in countries other than Japan, the United States and Europe, and Japan needs to vigorously implement its development, carefully discerning situations outside Japan.

Photo: Vice President Tanaka of ISTEC delivering a lecture speech at ISIS-15

The Summit meeting adjourned after agreeing to hold the next Summit meeting (ISIS-16) in the United States.

(Akihiko Tsutai, Director, International Affairs Department, ISTEC)

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Feature Articles: Technical Trends of Superconducting Digital Devices
- Trends of Superconducting Digital Device Technologies -

The development history of superconducting digital devices is old, dating back to the development of the so-called "Josephson computer" in the 1970s and 1980s. Beginning the second half of the 1990s, however, development has been focused on devices of the single flux quantum (SFQ) type. The most significant features of SFQ devices are fast clock operations from several tens of GHz to 100 GHz or more, which is one or two digits faster, and the power consumption per logic gate is about three digits lower compared with state-of-the-art silicon CMOS devices. These features are made possible because, unlike semiconductor devices, the devices are logic circuits that use pulses, the logic amplitude is small, mV or less, and superconducting wires that feature low losses can be used. Thanks to these features, SFQ devices are looked upon as devices with the potential to partially replace CMOS devices, which are beginning to exhibit limitations in high-speed performance enhancement due to heat, wiring delay and other problems, in the future.

In the development of digital systems using SFQ devices, the development of micro processors in the United States in the second half of the 1990s aimed at developing a peta-FLOPS computer was ahead of others. A processor chip that integrated about 70,000 Nb Josephson junctions was prototyped, but the chip did not function. In Japan, the development of infrastructure technologies including a device process that used Nb and Y-Ba-Cu-O high-temperature superconducting materials, SFQ circuit design technology and low-temperature fast packaging technology was strenuously undertaken in promotional research started in 1997 and sponsored by the former Science and Technology Agency and under two projects sponsored by the New Energy and Industrial Technology Development Organization (NEDO). These activities have earned Japan the position of world leader in device infrastructure technology. The on-going Superconductor Network Device Project sponsored by NEDO targeting Nb devices for high-end routers, servers and other large-scale digital systems and Y-Ba-Cu-O devices for A/D converters, samplers and analog/digital hybrid small-scale systems is beginning to demonstrate performance exceeding that of semiconductors on a parts level.

In the United States, HYPRES that is a venture enterprise with an old history spun out from IBM is at present acting as a center of development and is actively developing a wireless digital communication system receiving support from the military. Spurred by technology development achieved by Japan, the American government is being approached regarding a large-scale development program on superconducting computers, while the EU administration is being approached with an SFQ device technology development program centering on universities and national research laboratories as a national program. SFQ devices are also attracting attention as input and output circuits for quantum computers and signal processing circuits for electromagnetic wave sensor arrays. Research and development on them is being undertaken inside and outside Japan.

(Keiichi Tanabe, Director, Division of Electronic Devices, SRL/ISTEC)

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Feature Articles: Technical Trends of Superconducting Digital Devices - Development of Nb Integrated Circuit Fabrication Technology -

To date, many single-flux-quantum (SFQ) circuits having several thousand junctions have been developed using the SRL niobium (Nb) standard fabrication process composed of four Nb layers and Nb/AlOx/Nb junctions with minimum junction size of 2 μm square and critical current density of 2.5 kA/cm^2. They have been successfully operated at a clock frequency of approximately 40 GHz. However, to develop larger scale and higher speed SFQ circuits, a new Nb fabrication technology is required. We have been developing an advanced Nb fabrication process which is composed of Josephson junctions with a higher critical current density of 10 kA/cm^2 and planarized multiple Nb layers of more than six. [1)]

Figure 1 shows a cross-sectional SEM photograph of a device structure with nine planarized Nb layers fabricated by the advanced process. Excellent flatness is obtained for this multilayer structure using caldera planarization technology [2)] for all the Nb layers except the top layer. The multilayer structure enables shielding of the magnetic field caused by a bias current and free layout of PTL (passive transmission line) having a strip line structure over junctions, thereby allowing high integration.

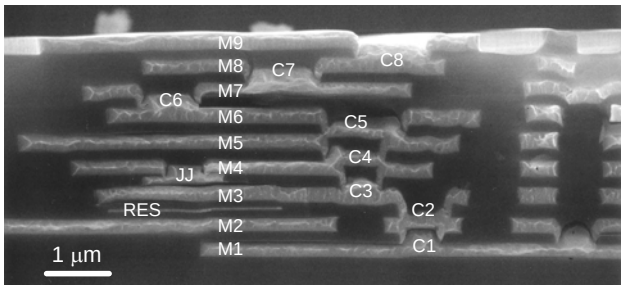


Fig. 1 Cross-sectional SEM photograph of a device structure with nine planarized Nb layers
Nb/AlOx/Nb junction (JJ), Mo resistance (RES) and contact (C_1-C_8). Nb film thickness: 300 nm, SiO_2 interlayer insulation thickness: 200 nm to 300 nm, Mo film thickness: 35 nm

A microphotograph of an 8-bit shift register fabricated by the advanced process is shown in Fig. 2. The shift register has a device structure of the advanced process composed of three Nb layers (M_2 to M_4 in Fig. 1). On-chip test results showed that this 8-bit shift register operated correctly at a clock frequency of up to 120 GHz. [3)] The maximum clock frequency of the shift register fabricated by the standard process is about 50 GHz. This means that operation that is twice as fast is accomplished, verifying the performance of the advanced process in terms of high speed.

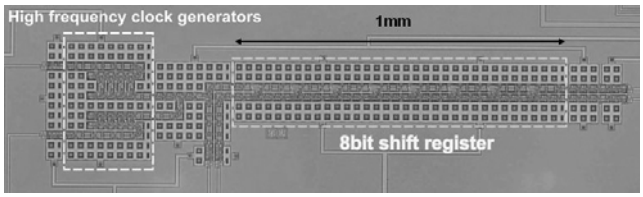
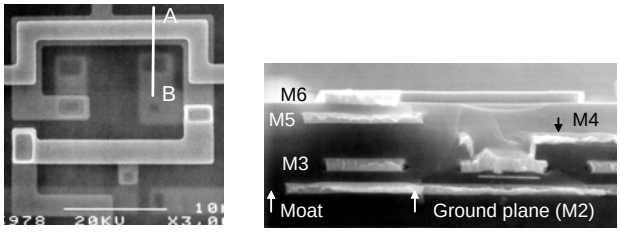


Fig. 2 Microphotograph of an 8-bit shift register fabricated by the advanced process (including clock generator). Operation at 120 GHz confirmed.

Four types of superconducting RAMs, with a storage capacity of 256 bits, 1 kbits, 4 kbits or 16 kbits were fabricated to evaluate the reliability and verify the effectiveness of the advanced process. Although the circuit configuration of these RAMs is almost the same as that of the previously developed one using conventional latching devices, [4)] the circuit parameters and layout design were modified based on the specifications of the advanced



(a) (b)

Fig. 3 (a) SEM photograph of memory cell (size: 22 μm × 22 μm), (b) Cross-section along A-B line of Fig. (a).

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fabrication process. Figure 3 shows the memory cell of the RAM fabricated by the advanced process with six Nb layers (M_1 to M_6 in Fig. 1), and a sectional SEM photograph of it. The memory cell is 22 μm square.

As an example, microphotographs of 4-kbit and 16-kbit RAMs are shown in Fig. 4. At present, correct operations with bit yields of 100 % for a 256-bit RAM (2,544 junctions), 99.8 % for a 1-kbit RAM (7,392 junctions) and 96.7 % for a 4-kbit RAM (23,488 junctions) are verified. Through this verification, we confirmed that evaluations using the RAMs were effective at detecting defects due to the fabrication process. The effectiveness of the advanced process with six Nb layers was also demonstrated in the RAM circuits including more than 10,000 junctions. Reliability of the advanced process will be improved by evaluating process defects using these RAMs.

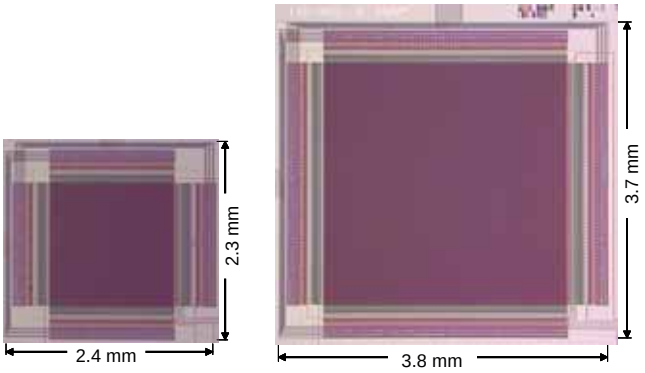

Fig. 4 Microphotographs of a 4-kbit RAM (23,488 junctions) and a 16-kbit RAM (80,768 junctions)

Acknowledgment: This work was supported by the New Energy and Industrial Technology Development Organization (NEDO) as a Superconductors Network Device Project.

References:

1) S. Nagasawa, K. Hinode, M. Sugita, T. Satoh, H. Akaike, Y. Kitagawa and M. Hidaka: *Physical C* **412-414** (2004) 1429-1436.
2) K. Hinode, S. Nagasawa, M. Sugita, T. Satoh, H. Akaike, Y. Kitagawa and M. Hidaka: *IEICE Trans. Electron.* **E86-C** (2003) 2511-2513.
3) H. Akaike, T. Yamada, A. Fujimaki, S. Nagasawa, K. Hinode, T. Satoh, Y. Kitagawa and M. Hidaka: *Supercond. Sci. Technol.* **19** (2006) S320-S324.
4) S. Nagasawa, Y. Hashimoto, H. Numata and S. Tahara, *IEEE Trans. Appl. Superconduct.* **5** (1995) 2447-2452.

(Shuichi Nagasawa, Low-temperature Superconducting Device Laboratory, Division of Electronic Devices, SRL/ISTEC)

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Feature Articles: Technical Trends of Superconducting Digital Devices - Evolution of Circuit Design and Packaging Technologies Targeting SFQ Switch -

Even in these times of large-capacity network equipment by photonic technology, complex processing such as control needs to be performed electrically. Considering data processing at a transmission speed of 40 Gbps or faster used in future large-capacity networks, the power consumption of the entire equipment may exceed the cooling limit due to a very large volume of hardware caused by parallel processing, because clock frequency of CMOS circuits are much slower than the processing clock. Realization of a single-flux-quantum (SFQ) switch, with which ultra-high speed and low power consumption can be accomplished simultaneously, is awaited to solve these problems. The Superconductivity Research Laboratory (SRL) is developing circuit design and packaging technologies to realize an SFQ switch.

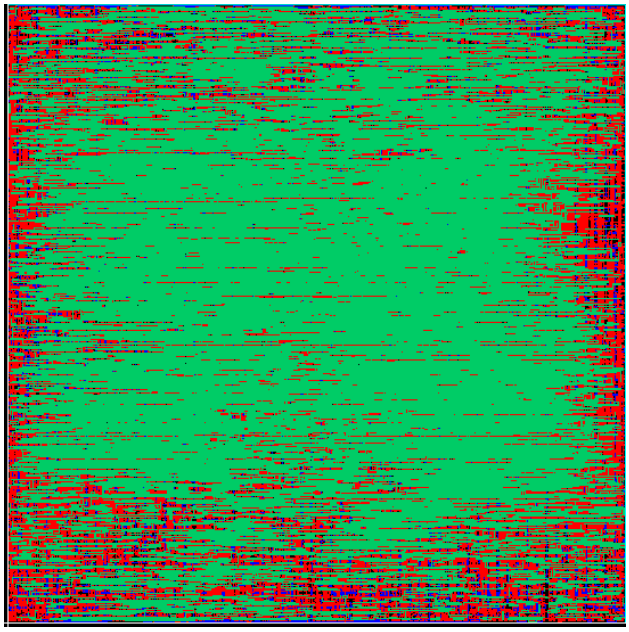

Fig. 1 8-bit RISC processor laid out by an automatic design tool

In circuit design technology, a top-down automatic design tool for SFQ circuits was developed. This tool automatically generates a physical layout of an SFQ circuit by preparing a logic circuit diagram matching SFQ circuit characteristics from a circuit specification written by a logic description language, by laying out each gate matching this logic circuit diagram and by connecting them by superconducting wiring called PTL. Operations of prepared SFQ circuits are verified by a simulator and their performances are forecasted. The logic description language is the same as that used in CMOS circuit design. Even those semiconductor designers who are not familiar with superconductivity can design large-scale SFQ circuits. Fig. 1 shows a layout of an 8-bit RISC (reduced instruction set computer) processor designed from CMOS logic description using this tool. The layout of an SFQ circuit that uses about 400,000 Josephson junctions was prepared in about 12 hours including operation verification. Clocks that are estimated by simulation are 27.6 GHz, greatly surpassing semiconductors in performance.

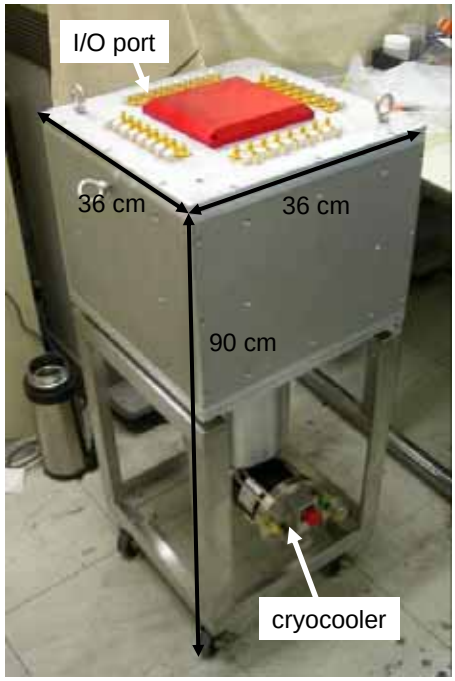

Fig. 2 Full view of widebande cryo-temperature subsystem

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In packaging technology, a device to exchange as many as 32 high-speed signals (10 Gbps) between an SFQ circuit operating at a liquid helium temperature (up to 4 K) and semiconductor apparatus in a room-temperature environment was developed. An experiment to test the operation of this device was successful. A full view of the newly developed device, the "wideband cryo-temperature subsystem," is shown in Fig. 2. Although a separately installed compressor is needed, the footprint including a refrigerator is compact, 36 x 36 x 90 cm. By connecting to a connector located in the top part of this device, input to and output from the SFQ circuit can be performed. An operation test using this device verified that a 10-Gbps electric signal is correctly output after being processed by the SFQ circuit. Values obtained in measurement of the bit error rate (BER) of the device were those on the 10^{-13} mark, adequate for use in communications.

These circuit design and packaging technologies are likely to accelerate the development of an SFQ switch. T This work was supported by the New Energy and Industrial Technology Development Organization (NEDO) as Superconductors Network Device Project.

(Mutsuo Hidaka, Director, Low-temperature Superconducting Device Laboratory, Division of Electronic Devices, SRL/ISTEC)

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Feature Articles: Technical Trends of Superconducting Digital Devices - Evolution of SFQ Processor Technologies -

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The microprocessor has the most complex structure among digital circuits and is a buildup of high-level technologies involving architectures, OS and a compiler. The microprocessor has been supported by CMOS technology that features low power consumption and high integration. CMOS technology seems to be progressing smoothly with all sails set. Nevertheless, its power density is approaching 100 W/cm^2, which is the limit for air cooling, and the operating frequency of the microprocessor is determined by the delay time of long wiring, instead of logic gates. A shadow has fallen on its high-speed performance. As these problems of the CMOS IC emerge, SFQ circuits that essentially feature high speed and low power consumption are again being spotlighted. Unlike semiconductor circuits, however, signals of SFQ circuits are impulsive and almost all logic gates require a latching function to store arrivals of signals. This latching function has been an obstacle to high speed for circuits that have a feedback part as in microprocessors. Furthermore, basically, wiring is communication from one output port to one input port, and the method of configuring circuits such as micro architectures has had to suit SFQ circuits.

A group led by Nagoya University and Yokohama National University has solved these problems one by one in the project “Development of Low-power-consumption Superconducting Network Devices” sponsored by the New Energy and Industrial Technology Development Organization (NEDO). The largest topic recently is probably the development of a 50-Gbps multicast passive wiring technology capable of transmitting data from one output port to a maximum of four input ports. This development has further accelerated small footprints and high speed. The use of circuit architectures that are suitable for SFQ circuits has expanded. A one-hot encoding technology suitable for pipeline processing that is essential for high speed was devised for the controller, while a dichotomous deterministic technology suitable for stream processing was devised for the instruction decoder unit and a status transition design method was devised for the arithmetic and logic unit (ALU) for logical operations without a feedback unit.

Figure 1 shows an SFQ microprocessor of the largest scale so far that succeeded in verification of operation. Designed using the CONNECT cell library developed jointly by SRL and NICT, the microprocessor was fabricated by the standard process of SRL, integrating about 11,000 Josephson junctions. The microprocessor employs a forwarding architecture that enhances processing efficiency by the cascade connection of two ALUs, and pipeline processing in four stages is used. The ALUs process bits at 20 GHz, capable of processing 1.5 Giga cycles per second at a peak

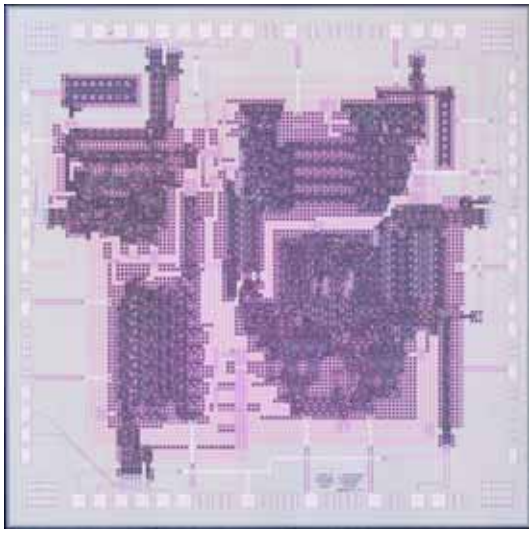

Fig. 1 SFQ microprocessor CORE1β that succeeded in operation verification

value. The number of instructions is small and the data length is short, but the number of processing cycles is almost the same as that of regular microprocessors. The power consumption of the microprocessor was 3.3 mW. This value is superior compared with semiconductors even when the input power of the refrigerator is taken into consideration, suggesting the potential ability of the SFQ microprocessor. A new architecture that overcomes the low data transfer ability between the memory and processor, which has been a bottleneck in configuring the supercomputer, has been devised recently. Details of this new architecture will be reported in the future; however, this architecture is blowing a new wind in SFQ circuitry application. Thus viewed, microprocessors of SFQ circuits are steadily making advances and a great leap is anticipated hand in hand with advances in integration technology.

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Advances in Fabrication and Design Technology for High-temperature SFQ Circuits
- Verification of High-speed Performance of Flip-Flop Element Circuits and Application to Functional Circuits -

The features of SFQ (single-flux-quantum) circuits that use high-temperature superconducting materials are high-temperature operation at 30 to 40 K and high-speed operations at several tens of to one hundred GHz. The circuit has a junction that uses the edges of an electrode film called ramp-edge junction. A fine junction area of less than 1 μm^2 and a high critical current density (J_c) can be accomplished, achieving high-speed operations without reducing the junction width to the order of submicrons.

Critical currents on junctions integrated into SFQ circuits need to be kept at a fixed value to operate SFQ circuits formed on an oxide thin film such as $YBa_2Cu_3O_{7-x}$. Flatness of the electrode film is essential for a uniform critical current distribution. The Superconductivity Research Laboratory (SRL) formed the oxide multilayer films, namely, three superconducting films including two junction electrode films and a magnetic shielding film, in addition to two insulating layers, by sputtering and other methods. After thoroughly examining film deposition parameters and minutely controlling them, the surface unevenness was improved to 1 nm with multilayer films exceeding 1 μm in total film thickness. On the other hand, the critical current was found to fluctuate by various circuit patterns other than the junction width such as the sizes of the base electrode.

A design used to trim sizes and shapes by separating the base electrode film for each junction found that the critical current can be adjusted only by the junction width. The critical current (J_c) distribution of superconducting junctions inside the circuit was discretely measured one by one. As a result, J_c dispersions were reduced to 8 % by modifying the circuit design, compared with 27 % with a toggle flip-flop of the conventional structure.

A variety of SFQ circuits were fabricated using these fabrication and design technologies. High-temperature operations of up to 60 K were confirmed with SFQ element circuits comprising 20 to 30 junctions such as set-reset, flip-flop, confluence buffer, toggle flip-flop and inverter circuits. The toggle flip-flop circuit especially achieved a frequency devider operation frequency of 360 GHz at 8 K and of 210 GHz at 41 K. (Fig. 1) Additionally, as a basic circuit for the next stage of elementary circuits, a 1:2 switching circuit provided with one input signal line, two clock signal lines and two output signal lines was

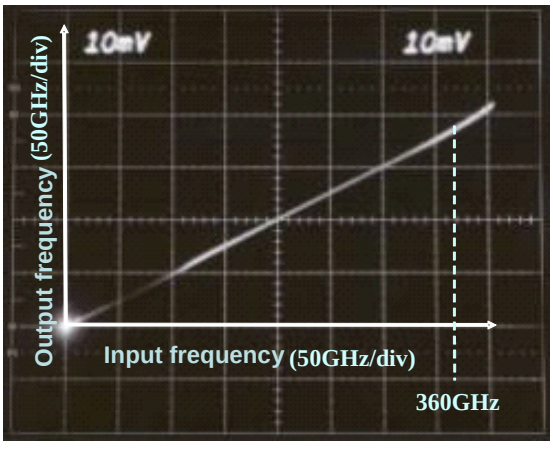

Fig. 1 Frequency divider characteristic of toggle flip-flop
(The operating frequency region is where the ratio between the input frequency and output frequency is in the range of 2:1.)

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fabricated. Logic operation at a temperature of 50 to 60 K was confirmed (Fig. 2). SRL plans to develop more functional SFQ circuits such as a 1:2 demultiplexer combining a toggle flip-flop and a switch circuit in the future.

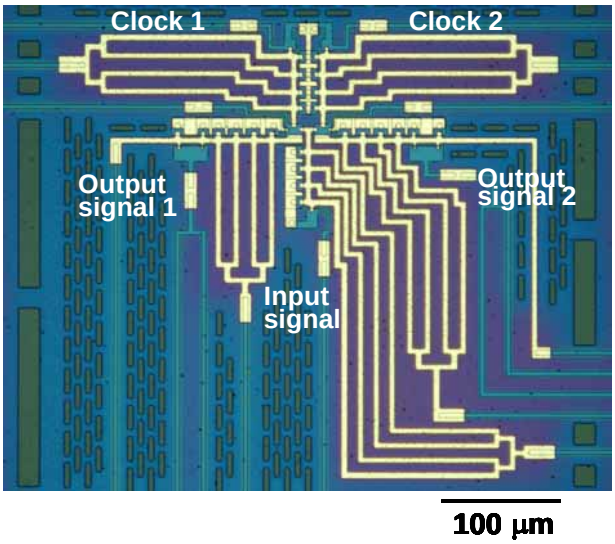

Fig. 2 The 1:2 switch circuits that verified logic operation

(Yoshinobu Tarutani, Division of Electronic Devices, SRL/ISTEC)

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Feature Articles: Technical Trends of Superconducting Digital Devices - Evolution of High-temperature SFQ Sampler and A/D Converter Technologies -

High-temperature superconducting devices can be cooled by a compact cryocooler, and then the systems can be downsized. As one of the application, HTS filters using passive devices are already on the market in the United States. In Japan, R&D is being undertaken for their commercialization. On the other hand, research of SQUID (superconducting quantum interference device) systems and THz wave detectors using active junctions (bicrystal junctions) is being carried out and several SQUID systems are commercialized.

SRL/ISTEC and Advantest Research are conducting R&D of an ultra-fast HTS sampler with fifteen junctions (ramp-edge junctions) as part of the Project for Development of Low-power-consumption Superconducting Network Devices. Both of an electrical signal HTS sampler and an optical input one are being developed. The latter one can input signals through optical fiber with almost no losses and small heat inflow. Then, a high-speed photodiode (UTC-PD: uni-traveling-carrier photodiode) operating more than 300 GHz can convert optical signal into electrical signal for the sampler chip. [1)] In the early stage of the project, low-temperature operation of the UTC-PD was verified. R&D to use this UTC-PD for the input of high-frequency signals is being carried out. Since photo diode modules on the market were not applicable to the sampler because they use magnetic materials are not capable of sampler operation, a special non-magnetic monolithic optoelectronic sampler module consisting of a UTC-PD and sampler chip was developed in cooperation with NTT Electronics Corporation. (Fig. 1) So far, waveforms of up to 20 GHz have been observed by this monolithic optoelectronic module. (Fig. 2) By improving the sampler chip reproducibility and the optical module for low temperature operation, a band in excess of 100 GHz can be anticipated. The development of a cooling system and measuring system for samplers using a compact cryocooler is also underway. Efforts are currently being made to develop a portable HTS sampler system.

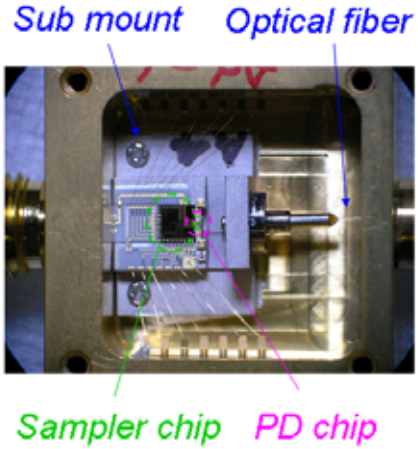

Fig. 1 Photo of monolithic optoelectronic module

In the same project, R&D of a sigma-delta (Σ-Δ) analog-digital converter (ADC) is being undertaken by the Advanced Research Laboratory of Hitachi, Yokohama National University and SRL/ISTEC. Basically, in this system high bit accuracy can be obtained with one quantizer by over-sampling and noise shaping. R&D is actively being undertaken for application of this system to future software wireless communication and for other applications. Superconducting SFQ circuits will allow a high-speed sampling frequency surpassing the sampling frequency of a semiconductor with low

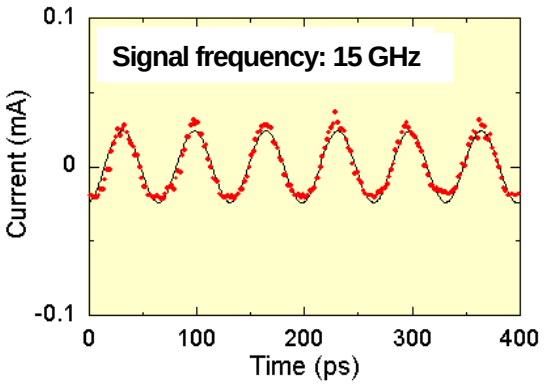

Fig. 2 Measured signal waveform

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power consumption, in addition to the natural quantization feature that they originally have. Such features can be accomplished by a relatively small circuit and are believed to be promising application fields for SFQ circuits. At present, R&D is being undertaken using LTS (Nb/AlOx/Nb junction) technology. However, HTS technology could be applicable in the future. The group is developing a hybrid system whereby a front-end circuit of a low pass type that has a quantizer with an integrator called a Σ-Δ modulator is built by superconductors and a back-end circuit whose main component is a decimation filter is built by semiconductors. (Fig. 3) The front-end part has produced an almost ideal power spectrum characteristic (noise shaping of 6 dB/oct) and performance of SINAD = 77 dB (ENOB = 12.5 b) at sampling frequency fs = 16 GHz and at bandwidth BW = 10 MHz. (Fig. 4) At present, operation at fs = 20 GHz is targeted for the entire system including the back-end circuit. As a good example of a Σ-Δ ADCs using superconducting technology for both the front-end and back-end circuits, R&D of a Σ-Δ ADC system is underway to digitize a very large volume of detection signals from a detector array of X-ray/THz called STJ (superconducting tunnel junction) cooled to below 1 K by a superconducting ADC at a cryogenic temperature. Hypres Inc., a venture company in the United States, has developed a prototype system of a low-pass ADC housing a 4-K cryogenic cooler and other units in a 19-inch rack. The system operates at fs = 11.52 GHz (performance of the chip itself is BW = 10 MHz, SINAD = 83 dB, @fas = 20 GHz). Furthermore, R&D is now underway for low-pass and band-pass ADCs for the development of direct conversion digital radio systems for military and consumer applications in the future.

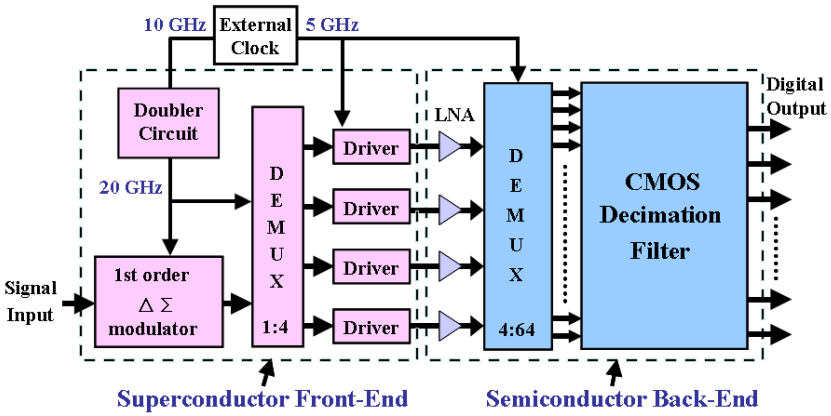

Fig. 3 Configuration of a hybrid ΣΔADC

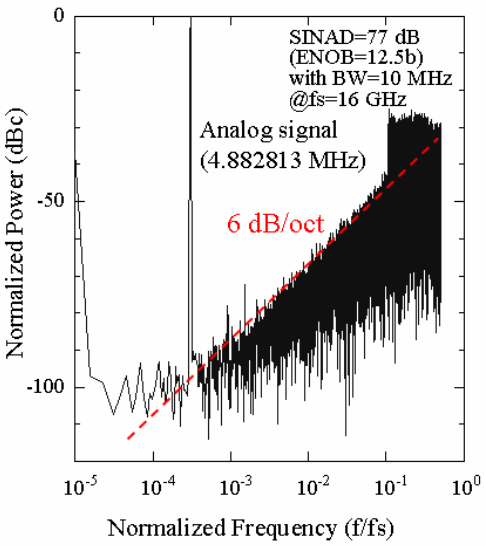

Fig. 4 Spectrum obtained

References:

1) Hideo Suzuki: *Superconductivity Web21*, p.3, Oct. 2005

(Hideo Suzuki, Division of Electronic Devices, SRL/ISTEC)

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Patent Information

Introduction of Published Unexamined Patents in the 2nd Quarter of Fiscal 2006

The following are ISTEC's patents published from July through September, 2006. For more information, access the homepage of the Patent Office of Japan and visit the Industrial Property Digital Library (IPDL).

1) Publication No. 2006-196604 "Superconducting Coil"

This invention relates to the structure of a superconducting coil using multilayered superconducting wires having a subdivided superconducting layer in plural slits. In this invention, the secondary parallel conductor is constructed by arranging these wires in parallel line and the tertiary parallel conductor is made by stacking these secondary parallel conductors in multiple layers. Finally, the tertiary parallel conductor is wound along the coil axis on the outer periphery of the coil spool. The tertiary parallel conductor having a lot of filamentary conductors, can easily realize a large-current coil, and the alternative current losses are also reduced by using the subdivided filamentary conductors in slits. By providing transposition between the superconducting wires in the secondary parallel conductor, the alternative current losses caused by a vertical magnetic field can be extremely reduced. Furthermore, by substituting a normal metal conductor for one of the superconducting wires in the secondary parallel conductors, the tolerance for the over-current can be strengthened.

2) Publication No. 2006-222314 "Superconducting Multilayered Article and Manufacturing Method thereof, Josephson Junction Device and Electronic Device"

This invention relates to a superconducting multilayered article with mercury superconducting films, to a manufacturing method thereof, and to Josephson junction and electronic devices having the superconducting multilayered article. The superconducting multilayered article related to this invention is sequentially stacked with the first mercury superconducting film on a substrate, an insulating film on the first superconducting film, and the second mercury superconducting film on the insulating film. The composition of the first and the second mercury superconducting films are formulated in (Hg, Re) $X_2CaCu_2O_y$ or (Hg, Re) $X_2Ca_2Cu_3O_y$ where "X" is Ba or Sr, and the insulation film is selected from CeO_2, $SrTiO_3$, $(LaAlO_3)_{0.3}$ - $(SrAl_{0.5}Ta_{0.5}O_3)_{0.7}$ (namely LSAT) and $(SrAl_{0.5}Ta_{0.5}O_3)_{0.7}$ (namely SAT). Using these material compositions, an insulation film with good crystal orientation can be deposited by heating the first superconducting film from 300 to 600 °C in an oxygen atmosphere without deteriorating the characteristics of the first superconducting film. Furthermore, the second superconducting film can now also be deposited on the foregoing insulating film with good orientation. All these films are grown epitaxially and the multilayered article is suitable in realizing a superconducting junction device and an electronic device of good quality and performance.

3) Publication No. 2006-252717 "Configuration of Superconducting Random Access Memory"

This invention relates to the configuration of large-scale superconducting RAM operating at a high speed and with very little power consumption. Number of memory cell blocks essentially increase in the scaling-up of the RAM. However, this causes increasing of the load in the driver circuit and sense circuits, making the high speed operation and low power consumption difficult. In this new superconducting RAM configuration, the drive lines accessing the memory cell blocks such as bit-lines and word-lines, are divided into several blocks as well as sense-lines. Signal propagations within the block are carried out by the internal block signal propagation circuits which have the driver circuits of the level-type signal with large

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driving capability, and superconducting passive transmission lines comprising SFQ devices are used for signal propagation between blocks that are separated by a long distance. This new configuration and the use of SFQ devices in the signal propagation circuits among blocks have enabled high-speed operation and ultra-low power consumption.

(Katsuo Nakazato, Director, Research and Development Promotion Division, SRL/ISTEC)

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Standardization Activities

Topics in November

- 2nd IEC/TC90 Superconductivity Panel Discussion in Seattle, USA -

IEC/TC90 sponsored the second panel discussion on IEC/TC90 superconductivity standardization in Seattle, U.S.A., on August 30 2006. Dr. L. Cooley of Brookheaven National Laboratory (BNL) acted as secretary. The panel discussions focused on current leads for superconducting equipment and apparatus and superconducting power cables.

The panel discussion was held as a satellite meeting during the Applied Superconductivity Conference 2006; ASC 2006 was held in Seattle, USA, from August 27 to September 1, 2006.

The following information was provided and the following topics were discussed during the panel discussions.

1) Representing the sponsor, Dr. Cooley of BNL, who acted as master of ceremonies, delivered an opening address and the purposes of the conference.

2) Information was provided by the following panelists.

◊ Dr. L. Goodrich of the National Institute of Standards and Technology (NIST) of America introduced standardization activities and procedures. Dr. Goodrich expressed the view that standardization should originally target those products that are technically mature and that further technological evolution should be expected with HTS.

◊ Dr. Kozo Osamura suggested that a great evolution can be expected for the superconductivity market in 2020 and that demonstrating superconductivity-applied equipment and apparatus is being carried out one after another. In superconductivity standardization activities, more international standards (IS) for glossaries and test methods are being established and maintained, and Dr. Osamura proposed that it was probably a good time to begin standardization relating to products such as general requirements as the next standardization targets.

◊ Prof. Takakazu Shintomi reported that standardization of general requirements on current leads was approved at the TC90 Kyoto Conference. Prof. Shintomi explained that the current status was a WG inaugurated within IEC/TC90 to study NWIP.

◊ Mr. Ken-ichi Sato reported the current status of standardization of superconductivity-applied equipment and apparatus. Power cables were taken up as an example of R&D activities on superconducting equipment and apparatus that are being undertaken. Characteristics and structures required of power cables from the standpoint of achievements and technology in the world of R&D were introduced. Mr. Sato stressed the necessity of standardizing long-length high-temperature superconducting wires as their product elements.

◊ Mr. Shin-ichi Mukoyama made announcements on features of evaluation of the characteristics of HTS power cables. Mr. Mukoyama overviewed the power situation and needs regarding superconducting cables in the world. A study on the economic effects of power cables and specific requirements for commercialization in Japan were reported.

3) Discussions

◊ At the beginning, Dr. Cooley explained the procedures for the discussions.

◊ As a general discussion, a question was asked: “In the first place, is standardization of superconductivity necessary?” Some people voiced concern that standardization activities might obstruct R&D activities by laboratories, universities, enterprises and other organizations. Dr. Cooley and others explained that standardization included the unification of superconductivity glossaries and test and evaluation methods.

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The panelists agreed that they had no objection to this part.

◊ Prof. D. Larbalestier of NHMFL/FSU made an academic proposal on new critical current standardization for HTS tape wires. The proposal proposes to evaluate the critical current characteristic of superconducting wires by measuring pinning force at 1T to simplify measurements without depending on kinds of superconducting wires. Some participants expressed the views that the critical current probably had to be evaluated by at least more than two magnetic fields and by a 3-dimensional characteristic of a temperature, magnetic field and current and that information of n-value was also important.

◊ Dr. Kozo Osamura explained about past activities on standardization of the critical current in low temperature superconductivity and described a method to measure and evaluate the critical current of NbTi wires. Dr. Osamura mentioned that n-value had a large error, 30 %, and that the value was used as a reference value.

◊ The necessity of evaluating AC losses based on the experience in low temperature superconductivity was pointed out regarding the method to measure AC losses of high temperature superconductors. It was reported that standardization was in progress in Japan on VAMAS activities.

◊ Regarding measurements of characteristics of high temperature superconducting wires, it was mentioned that enterprises wished to have standardization of a simple, low cost and high reliability measurement method. The participants pointed out the necessity of especially measurement methods for critical current, AC losses, n-value and other parameters, as well as for a technique to evaluate quality of long-length wires.

◊ Regarding standardization of current leads, the participants said that they understood the standardization activities in the past and that they had no objection to moving on to NWIP (New Work Item Proposal) for standardization as approved for the four countries that participated in the 10th IEC/TC90 held in Kyoto on June 8, 2006. The participants agreed that future discussions were needed on the necessity for a method to evaluate invasive heat in common test methods and other matters on standardization, that standardization should not hamper R&D by enterprises, laboratories and other bodies and that efforts should be made to obtain concurrence of many people.

4) Panel discussions in future

In conclusion, it was agreed that panel discussions like the discussion in Seattle were very useful in gaining understandings of many more people and in pursuing appropriate standardization as standardization activities and that similar opportunities should be arranged in the future also.

This report on the 2nd IEC/TC90 Superconductivity Panel Discussion in Seattle has been compiled based on information provided by Kozo Osamura, Toshiyuki Mito, Ken-ichi Sato, Takakazu Shintomi, Shin-ichi Mukoyama, L. Cooley and other persons.

- Prof. Satoru Murase, Dr. Kikuo Itoh and Dr. Yasuzo Tanaka Awarded IEC-1906 Award -

Prof. Satoru Murase, Okayama University Graduate School, Dr. Kikuo Itoh, National Institute for Materials Science, and Dr. Yasuzo Tanaka, International Superconductivity Technology Center (ISTEC), were awarded the 1906 Award of the International Electrotechnical Commission (IEC).

The awarding ceremony was held in the JA Building in Otemachi, Chiyoda Ward, Tokyo, on Friday, October 13, 2006. As part of the commendation ceremony for the 2006 Industrial Standardization Award sponsored by the Ministry of Economy, Trade and Industry, the awards were awarded concurrently with the commendation ceremonies for the Industrial Standardization Activity Award, Standardization Contribution Award and Standardization Senryu (witty 17-syllable verse) Prize. Councilor Ryutaro Matsumoto, Minister's Secretariat, Ministry of Economy, Trade and Industry, Dr. Seiichi Takayanagi, former

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president, IEC, Vice President Hidesuke Shoda, vice president, JISC (Japanese Industrial Standards Committee), Ms. Mariko Sato, director, Secretariat, Shufuren ("Housewives Federation": a consumer organization), and Dr. Mitsuru Imagawa, president, Nissenkyou (All Japan Senryu Association), were invited to the ceremonies. Awards and prizes were bestowed upon 25 persons who made distinguished standardization services, two organizations for their contribution to standardization, 21 recipients of the IEC-1906 award, five persons for making contributions to standardization selected by the Japanese Standards Association and two recipients of the Standardization Senryu Grand Prix.

Among the 21 persons honored with the IEC-1906 Award, three persons related to superconductivity received the awards for the following reasons.

Prof. Satoru Murase, Okayama University Graduate School

For contribution to plan development and consensus forming on IEC 61788-10 (critical temperature test method) and IEC 61788-1 (DC critical current test method) and for services provided in playing a major role in technical field as a WG11 convener.

Dr. Kikuo Itoh, National Institute for Materials Science

For services provided in playing a major role in technical field in WG3, WG7 and WG9 on standards development and consensus forming at IEC/TC90.

Dr. Yasuzo Tanaka, International Superconductivity Technology Center (ISTEC)

For services provided in contributing to development of all international standards of IEC/TC90 as a co-convener of WG7 and as the domestic secretary of IEC/TC90 Japan Committee.

Photo: Commemorative photographing of award recipients.
Rear row - Dr. Kikuo Itoh (on left), Dr. Yasuzo Tanaka (second person from left)
Front row - Prof. Satoru Murase (second person from right)

(Yasuzo Tanaka, Director, Standardization Department, ISTEC)

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