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Superconductivity Web21

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What's New in the World of Superconductivity (November)

Power

American Superconductor Corporation (November 9, 2005)

American Superconductor Corporation (AMSC) has reported their financial results for their fiscal second quarter ending September 30, 2005. Revenues increased by 14% to US $10.9 million, compared with $9.5 million for the same period in the previous fiscal year. The net loss was $6.8 million, compared with $4.1 million for the same period in the previous fiscal year. AMSC ended the quarter with cash, cash equivalents, and short- and long-term investments of $74.5 million and no long-term debt. The company received $5.2 million in new orders and contracts during the second quarter, bringing its total backlog of orders and contracts to $18.4 million. AMSC updated its revenue visibility for fiscal 2006 to approximately $46 million. "Taking into account the orders and contracts that we anticipate closing this quarter, in addition to our current revenue visibility, we are now targeting $55 to $60 million in revenues for fiscal 2006," said Greg Yurek, president and CEO of AMSC.

AMSC expects to complete a "substantial number of additional orders" for power electronic systems in their fiscal third and fourth quarters. The status of these orders should be confirmed by the end of the calendar year. Two new contracts from the U.S. Navy for ship propulsion motors and generators are also expected during the fiscal fourth quarter. Furthermore, two new superconductor projects are anticipated to begin next year; as part of the "Power Delivery Research Initiative" (PDRI), the DOE plans to develop a controllable, alternating current cable system and a direct current cable system. These new projects are expected to provide a substantial revenue opportunity for AMSC.

Source:
"American Superconductor Reports Fiscal 2006 Second Quarter and Six-Month Results"
American Superconductor Corporation press release (November 9, 2005)
http://phx.corporate-ir.net/phoenix.zhtml?c=86422&p=irol-newsArticle_Print&ID=780720&highlight

American Superconductor Corporation (November 14, 2005)

AMSC has announced an order for a 40 MVAR Dynamic VAR Compensator (DVC™) to be installed in an Icelandic power transmission grid operated by Landsnet, an independent power transmission company. DVC systems are large-scale, transmission-level reactive power solutions built on AMSC's patented D-VAR platform. The DVC system will be installed in a substation located near a new aluminum plant that will add an electrical load of approximately 540 MW to the power grid. The DVC will provide dynamic voltage control and regulation, and will support overall power network stability. AMSC expects to ship the system in the summer of 2006 for installation and commissioning in the autumn of 2006. Terry Winter, AMSC's executive vice president and chief operating officer, commented, "The Landsnet installation is an excellent example of how critical dynamic voltage regulation is in ensuring reliable and efficient transmission of electricity for both industry and consumers."

Source:
"American Superconductor Receives Order for Dynamic VAR Compensator (DVC(TM)) System from Grid Operator in Iceland"
"American Superconductor Reports Fiscal 2006 Second Quarter and Six-Month Results"
American Superconductor Corporation press releases (November 9 and 14, 2005)
http://phx.corporate-ir.net/phoenix.zhtml?c=86422&p=irol-newsArticle_Print&ID=782182&highlight
http://phx.corporate-ir.net/phoenix.zhtml?c=86422&p=irol-newsArticle_Print&ID=780720&highlight

American Superconductor Corporation (November 16, 2005)

AMSC has finalized a contract amendment with the U.S. Department of Energy (DOE) regarding the Long Island Power Authority (LIPA) cable project. Under the terms of the amendment, the DOE will increase its share of the total approved budget (US $46.9 million) by $8.3 million. This additional sum will be added to AMSC's backlog in fiscal third quarter 2006. AMSC plans to ship the final 89,600 meters of HTS wire required by the project to the cable manufacturer, Nexans, during the present fiscal quarter. The cable is on schedule for installation in the LIPA grid and is expected to become operational in September 2006.

Source:
"American Superconductor Awarded Contract Amendment by Department of Energy for Long Island Power Authority Cable Project"
American Superconductor Corporation press release (November 16, 2005)
http://phx.corporate-ir.net/phoenix.zhtml?c=86422&p=irol-newsArticle_Print&ID=783511&highlight

Nexans (November 16, 2005)

Nexans will lead a consortium of Forschungszentrum Karlsruhe, the University of Hanover, EnBW Energie Baden-Württemberg AG and RWE Energy to develop an HTS fault current limiter (SCFCL) for use in 100-kV networks. The project will initially focus on the development of a single-phase SCFCL module for laboratory tests. Two three-phase prototypes will then be constructed for network trials by EnBW Energie Baden-Württemberg AG and RWE Energy. The SCFCL will utilize BSCCO 2212 superconductors manufactured by Nexans SuperConductors GmbH (a Nexans company based in Germany). The SCFCL will be based on the principle of "magnetic field triggering" developed in the previous CURL 10 FCL project. This design concept is expected to result in an economic breakthrough that may help to advance the application of superconducting FCLs by minimizing material requirements and reducing cooling costs.

Source:
"Nexans leads co-operative project to develop 110 kV superconducting fault current limiters "
Nexans press release (November 16, 2005)
http://www.nexans.com/internet/Content.nx?contentId=7175

American Superconductor Corporation (November 21, 2005)

AMSC has signed an agreement with the Korea Electrotechnology Research Institute (KERI) to become an international collaborator in Korea's Development of Advanced Power Systems by Applied Superconductivity technologies (DAPAS) program. AMSC will become the sole supplier of the 14 km of first-generation HTS wire required by the project. The company expects to ship the wire before the end of calendar 2005. AMSC will also provide technical assistance in the areas of cryogenics and transmission system engineering. LS Cable, a Korean cable manufacturer, will fabricate the 70-meter cold dielectric 22.9-kV, 1.26-kA cable, which will be installed in a live transmission grid. LS Cable will also produce the cryogenics system and the terminations.

Source:
"Korean Cable Demonstration Project Selects American Superconductor as Sole Supplier of High Temperature Superconductor Wire"
American Superconductor Corporation press release (November 21, 2005)
http://phx.corporate-ir.net/phoenix.zhtml?c=86422&p=irol-newsArticle_Print&ID=784925&highlight

American Superconductor Corporation (November 29, 2005)

AMSC has received a follow-on order for PowerModule-based wind turbine generator control systems from Windtec Systemtechnik GmbH, an Austrian supplier of large wind turbine components and

system technology. The PowerModule PM1000 power converters will be incorporated into 23 wind turbine generators, each rated at 1.5 MW, that Windtec plans to ship to China and Japan in calendar 2006.
Source:
"American Superconductor Receives Follow-on Order from Austrian Wind Turbine Supplier, Windtec, for Wind Turbine Generator Control Systems"
American Superconductor Corporation press release (November 29, 2005)
http://phx.corporate-ir.net/phoenix.zhtml?c=86422&p=irol-newsArticle_Print&ID=790689&highlight

MRI

Siemens Medical Solutions and Invivo Corporation (November 3, 2005)

Siemens Medical Solutions and Invivo Corporation have announced a strategic partnership to integrate Invivo's computer-aided-detection (DynaCAD) system with Siemens' MAGNETOM MRI systems for advanced breast MRI technology. The new systems will provide radiologists with more detailed information and streamline workflows through managing large volumes of images. Thomas Tynes, a director at Invivo Corporation, stated, "The addition of DynaCAD to the existing line of Siemens-certified Invivo breast MRI coils and biopsy systems provides a comprehensive, fully-integrated approach to breast MRI diagnostics and intervention."
Source:
"Siemens and Invivo Partner to offer Computer-Aided-Detection System for MRI"
Siemens press release (November 3, 2005)
http://www.medical.siemens.com/webapp/wcs/stores/servlet/PressReleaseView?langId=-1&storeId=10001&catalogId=-1&catTree=100005,13839&pageId=68590
Intermagnetics General Corporation press release (November 3, 2005)
http://www.igc.com/news_events/news_story.asp?id=173

Communication

Superconductor Technologies Inc. (November 2, 2005)

Superconductor Technologies Inc. (STI) has announced their fiscal results for their third quarter, ending October 1, 2005. Net revenues decreased by 46% to US $3.9 million, compared with $7.3 million for the same period in the previous fiscal year. Net commercial product revenues decreased by 50% to $3.1 million, compared with $6.1 million for the same period in the previous fiscal year. Government and other contract revenue totaled $865,000, compared with $1.2 million for the same period in the previous fiscal year. An ongoing focus on streamlining operations resulted in a reduction in the company's net loss, from $5.2 million for the same period in the previous fiscal year to $3.6 million in the presently reported fiscal quarter. As of the end of the third quarter, STI had a commercial product backlog of $950,000, with remaining minimum purchase commitments totaling $1.5 million under a general purchase agreement from one customer. During the third quarter, STI received net proceeds of 11.5 million dollars. The company has $18.8 million in working capital, including $14.9 million in cash and cash equivalents.

For the first nine months of 2005, total net revenues were $16.8 million, compared to $19.1 million for the first nine months of 2004. Net commercial product revenues for the first nine months of 2005 were

$14.4 million, compared to $13.8 million in the year ago period. STI recorded $2.4 million in government and other contract revenues for the first nine months of 2005, compared to $5.2 million for the first nine months of 2004. The net loss for the first nine months of 2005 was $11.2 million, compared to $19.9 million for the prior year's first nine months, which included restructuring expenses of $2.7 million, a non cash interest charge of $802,000 for warrants issued in connection with a bridge loan, and ISCO related litigation expenses of $438,000.

Source:
"Superconductor Technologies Inc. Announces Third Quarter 2005 Results"
Superconductor Technologies Inc. (November 2, 2005)
http://phx.corporate-ir.net/staging/phoenix.zhtml?c=70847&p=irol-newsArticle&ID=777426&highlight

ISCO International (November 3, 2005)

ISCO International (ISCO) has provided a financial update on its operations. ISCO's visualized revenue for their fourth quarter, based on shipped orders and orders expected to ship during the quarter, totaled US $0.6 million as of the end of October. This revenue is equivalent to the revenue for the entire fourth quarter of the previous fiscal year. John Thode, CEO of ISCO, commented, "While we didn't get off to as quick a start in Q4 as we would have liked, we are ahead of our Q3 pace and have visibility to a number of near-term opportunities. Having significantly improved the cycle time and efficiencies of our supply chain, we will also be prepared to fulfill orders we receive late in the year, a phenomenon we often see in our business as operators complete their budget cycle." The company recently completed an extensive commercial trial with a new customer, with excellent results. This success may lead to significant deployment over the next year.

Source:
"ISCO INTERNATIONAL PROVIDES FINANCIAL UPDATE FOR THE FOURTH QUARTER 2005 AND INVESTOR CALL INFORMATION"
ISCO International press release (November 3, 2005)
http://www.iscointl.com/

(Akihiko Tsutai, Director, International Affairs Department, ISTEC)

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Feature Articles : Advances in Superconducting Digital Devices
- Applications Expanding for Superconducting Digital Devices -

Superconducting digital devices have a long history, dating back to research and development on latching circuits typified by the so-called Josephson Computer in the 1970s and 1980s. Latching circuits are level logic circuits that use Josephson junctions (JJs) as active elements, but they represent voltage levels as either 1 or 0, just as semiconductor circuits do. Since their clock frequency in principle maxes out at several GHz, they were not able to surpass silicon CMOS devices that were rapidly advancing in the 1990s. The idea of logic devices using the magnetic-flux quantization characteristic of superconductivity originated in Japan in the 1970s, but since K. Likharev of the State University of New York announced a gate family dubbed rapid single-flux-quantum (RSFQ), it has been becoming the mainstream of superconducting digital device development. Such devices, commonly known as SFQ devices, represent both the state in which there is a magnetic flux quantum on the superconducting loop, and the state in which there is not, as 1 and 0 respectively. They employ JJs as switches and are characterized by so-called pulse logic in which a magnetic flux quantum propagates over the connected superconducting loop, while at the same time, a quantized voltage pulse signal (mV level) with a width of several ps travels through a superconducting wire. Owing to use of lossless superconducting wiring in addition to such characteristics as a small signal amplitude, high-speed switching, and pulse logic, the SFQ devices are the only ones that are capable of clock frequencies exceeding 100 GHz at the LSI level. Moreover, since SFQ devices are further characterized by low power consumption that is two or three orders of magnitude better than that of CMOS devices, the International Technology Roadmap for Semiconductors (ITRS) is considering them as the most promising new candidate for logic devices that will break through the silicon device limit that has finally come into view.

The primary applications envisioned for SFQ devices—listed starting from the lowest level of integration (JJs/chips) required—include measuring instruments, such as samplers and digital SQUIDs (20 to 100 JJs), analog-to-digital (A/D) converters for measuring or wireless communications (500 to 10^4 JJs), digital signal processors for radio astronomy and particle beam/nuclear physics measurements (10^5 to 10^6 JJs), switches for high-end network routers (10^5 to 10^6 JJs), and processors for servers and supercomputers (10^6-10^7 JJ). In Japan, which launched fundamental technology development for SFQ devices around 1997 or 1998 as a national project, circuit operation on the scale of about 10,000 JJs on low-temperature Nb circuits, and on the scale of 200 JJs even on high-temperature YBCO circuits made of complex materials, is becoming possible thanks to advances in process and design technologies. Thus the nation has reached a technology level that leads the rest of the world. At present, development is underway with an eye on demonstrating performance at the component level for medium-to-large-scale equipment, such as network routers, servers and A/D converters when using Nb circuits, and for small-to- medium-sized equipment, such as samplers that use small cryocoolers and A/D converter circuits when using oxide circuits. Connection with semiconductor devices and equipment operating at different environment temperatures and signal levels is essential to putting equipment and systems that use SFQ devices into practical use, and efforts are being particularly focused on developing a high-speed interface technology between several GHz and 100 GHz.

(Keiichi Tanabe, Director, Division of Electronic Devices, SRL/ISTEC)

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Feature Articles: Advances in Superconducting Digital Devices
- Current State of SFQ Packet Switch Circuits/Packaging Technology -

SFQ digital circuits are known for their high speed and low power consumption characteristics. Packet switch of future high-end router is considered as one of suitable applications for SFQ digital circuits. Packet switch is a kind of random logic circuits, so we have developed both fabrication technology and design methodology (EDA tools, cell library, and wiring). By using these developed technologies, a packet switch circuit and a switch scheduler circuit were designed and fabricated. Both circuits worked at 40GHz clock frequency. Figure 1 shows a photo of a packet switch chip. For realizing an SFQ subsystem, development of packaging technology is essential. As a first step, we have developed a 32-channel cryocooler system. Each channel speed is 10Gbps. Figure 2 shows a block diagram of the system. It consists of multi-chip module, high-speed multi-pin probe, cryogenic semiconductor amplifier, interconnection cables between room-temperature and low-temperature. We are now integrating whole elements, in which an attractive demonstration can be expected.

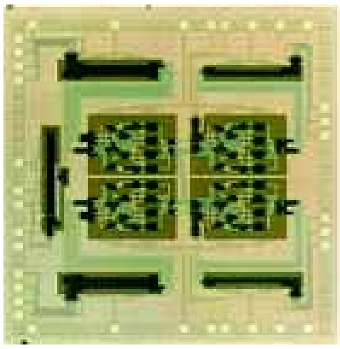

Fig. 1 Photo of 4x4 switch chip with a clock speed of 40 GHz.

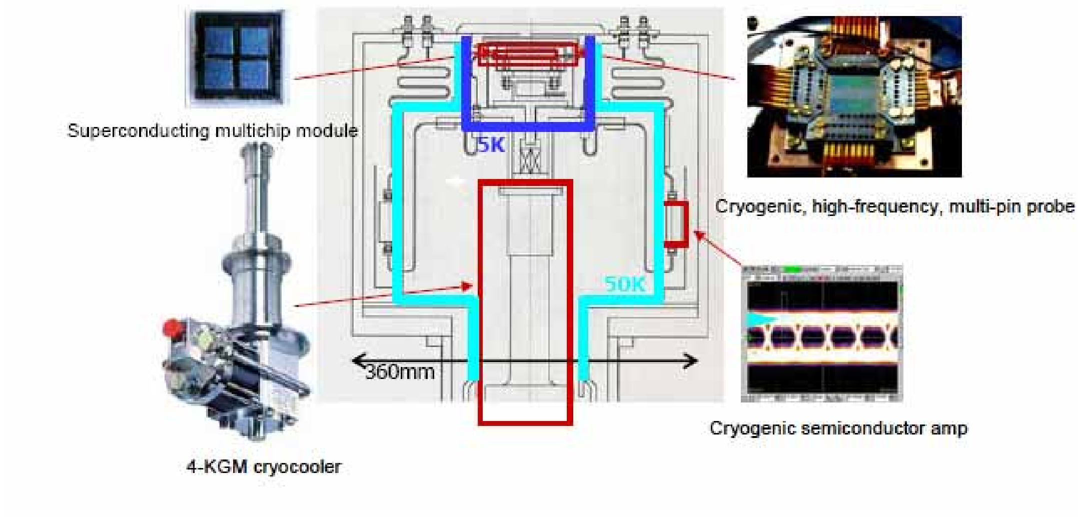

Fig. 2 Cryocooler system under development

(Shinichi Yorozu, Low Temperature Superconducting Device Laboratory, Division of Electronic Devices, SRL/ISTEC)

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Feature Articles : Advances in Superconducting Digital Devices
- Advances in Ultrahigh-Speed HTS Sampler Technology; Success in SFQ Pulse Observation Using an On-Chip Sampler -

The speed of measurement systems is being increased in order to develop high-speed devices and network systems. In April 2005, the commercialization of a 100 GHz-band sampling oscilloscope using semiconductor technology was announced. Even faster systems and electric current measurement systems using superconducting technology are expected.

Following S. M. Faris's proposal on the research and development of superconducting samplers at IBM in 1980, commercialization using LTS technology with He gas cooling was carried out at Hypres. Later, M. Hidaka of NEC conducted research and development on an HTS sampler using a cryocooler in an effort to produce a more practical system[1)]. Taking over his work, Superconductivity Research Laboratory has made research and development on a superconducting sampler that exceeded 100 GHz as part of its Low Power Consumption Superconducting Network Device Development Project starting in 2003. Following the observation of a 45-GHz waveform by the electric current input method reported in 2004[2)] that surpassed the previous maximum frequency of 20 GHz, the Superconductivity Research Laboratory also succeeded in observing a 50 GHz waveform with the voltage input method using the high-frequency module (Figure 1) of the superconducting sampler developed in cooperation with Advantest Laboratories[3)]. However, in the previously obtained results, the signal loss of coaxial cable, modules, and other items, and also jitter in the measurement system has made it difficult to assess whether superconducting sampler chips are really operating at a high speed.

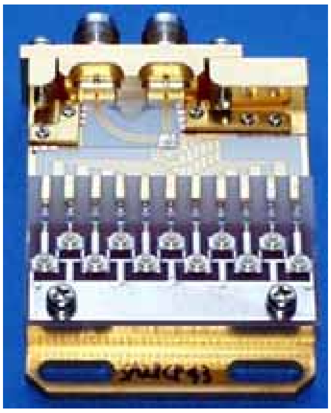

Fig. 1 High-frequency module

On-chip samplers that employ two single-flux quantum (SFQ) pulse generators as sampling pulse and signal pulse were prepared as one method to evaluate the high-speed performance of the chip itself. Then on-chip sampler circuits that measured SFQ pulses using the same SFQ pulses were designed and fabricated (Figure 2). The waveform observation of SFQ pulses with the HTS sampler was firstly succeeded by using a cryocooler to cool the chip to 40 K and then (Figure 3). The SFQ pulse width observed this time was about 10 ps. Based on this result, it was estimated that 100 GHz would be possible for the bandwidth of the chip itself, even using the current process technology (typical junction parameter I_cR_n = 0.7mV).

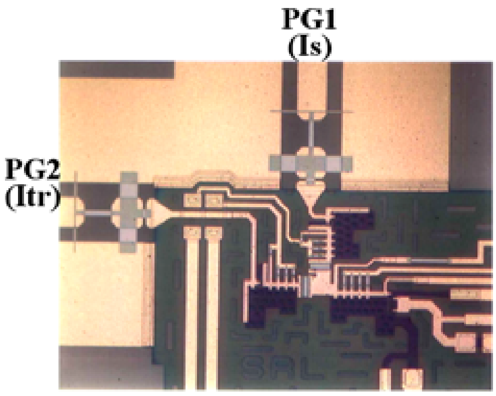

Fig. 2 Photomicrograph of on-chip sampler

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In addition, it is becoming clear that the jitter and thermal noise in the sampling pulse has an effect on the bandwidth of a sample from simulated results[4]. The performance can be increased by improving process uniformity, reproducibility, and measurement system to counteract such effects. Furthermore, the basic operation of a superconducting sampler using a cooled high-speed photodiode in the signal input section has been succeeded recently, which means a bandwidth of 100 GHz should be possible in the near future.

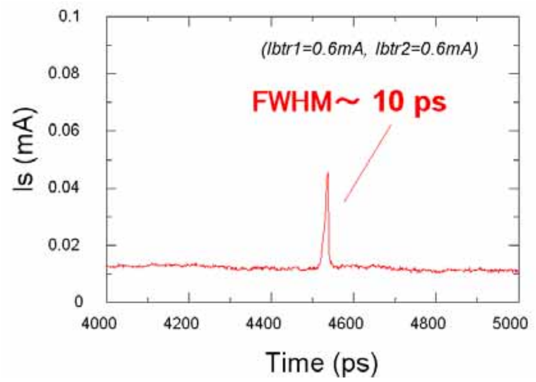

Fig. 3 Observed waveform of SFQ pulse

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1) M. Hidaka, M. Maruyama, and T. Satoh: IEICE (the Institute of Electronics, Information and Communication Engineers) Trans., Nov. 2003, pp. 1128-1135.
2) H. Suzuki: Superconductivity Web 21, Winter, 2005, p. 16.
3) H. Suzuki et al. Physica C 426-431, p.1643, 2005
4) M. Maruyama et. al., ISS2005 (Proceedings of ISS2005 to be published as a special issue of Physica C, 2006).

(Hideo Suzuki, Division of Electronic Devices, SRL/ISTEC)

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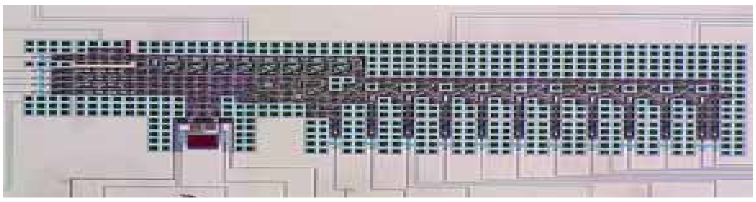
Feature Articles: Advances in Superconducting Digital Devices
- Advances in Analog/Digital Converters -

Akira Fujimaki, Professor
Graduate School of Engineering
Nagoya University

Ever since it was proposed that analog-to-digital converters (ADCs) using superconducting flux quantum (SFQ) circuits could be applied to software-defined-radio receivers, which are the next generation of radio communication technology, oversampling ADCs have been the mainstream of development. SFQ-ADCs can achieve a high precision not possible by other means, because they are capable of accurate negative feedback with a flux quantum unit and of high-speed operation of several tens of GHz. Although a digital RF receiver, which directly converts multiple radio signals simultaneously into digital values and then carries out demodulation and channel selection numerically, is known to be an ideal-like radio receiver having high flexibility, the speed and precision of an SFQ-ADC are necessary to satisfy the demand for the ADC that would be used there. In addition, the demand has been growing lately for an increased number of superconducting tunnel junctions (STJs) in a detecting system for x-rays and terahertz-waves. The idea of using SFQ-ADCs and SFQ-multiplexers in the multiplexing of output from each STJ also has been proposed, and the quick development of SFQ-ADCs is demanded strongly from the standpoint of the detecting system.

An oversampling ADC comprises a modulator on the first part and a decimation filter on the last part. The modulator must operate at an ultra fast speed, which makes the SFQ technology essential. Moreover, the decimation filter is a high-speed digital integrated circuit. This part can be implemented either using an SFQ circuit or using a semiconductor circuit after parallelizing the data and reducing the speed, each of which alternative has advantages and disadvantages. However, the former implementation, which enables SFQ circuits to have a variety of functions through digital signal processing, is thought to be beneficial when considering SFQ-ADCs made of Nb junctions. That is why we went forward with the development of ADC toward a multiple STJ detectors system. In addition, this was positioned as the first state of the development of a digital RF receiver. The photo shows the SFQ-ADC manufactured using Nb/AlOx/Nb junctions (NEC standard process). It has 807 junctions, and both the modulator and decimation filter are operated at a clock speed of 14 GHz by the built-in oscillator. In addition to employing magnetic coupling input to deliver high sensitivity, this ADC contains two quantizers to reduce external noise and improve the signal-to-noise ratio (SNR). Although the actually measured SNR is 7.5 bits in the 20 MHz band width, we know that the target value of 14 bits is possible after improving the decimation filter. Meanwhile, Hypres in the U.S. has already been getting measurements of 11.8 bits and has even succeeded in developing an ADC comprising 12,000 junctions in an effort to produce a digital RF receiver. We believe that there will be a strong demand for various performance enhancements for ADCs and for their actual use in systems.



Photomicrograph of ADC manufactured on a trial basis

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Feature Articles : Advances in Superconducting Digital Devices - Prospects for Post-CMOS Technology -

Nobuyuki Yoshikawa, Professor
Graduate School of Engineering,
Yokohama National University

Even CMOS technology, which has attained dramatic performance improvements through diminishing device dimensions, is now facing many difficulties. The main reason for this is that power consumption can not be further reduced due to the growing leak current that is making it difficult to lower threshold values and reduce gate oxide film. The increasing wiring delay that accounts for circuit operation time also invites worsening circuit performance. According the ITRS's roadmap, performance increases from CMOS technology can be expected up to the 22-nm generation planned for development in 2016. However, that will require the development of a variety of new technologies, such as strain silicon technology, insulator technology for high-dielectric gate, SOI technology, and technology for constructing 3D MOS. Furthermore, this is not a matter of simply developing a single technology but, rather, the performance in the roadmap will only be achieved by the gradual deployment of all the aforementioned technologies. Consequently, the development of CMOS technologies will require ever-increasing efforts and investments.

Meanwhile, the roadmap introduces a number of new logic device technologies (Table 1) as candidates for post-CMOS technologies. Except for superconducting flux quantum (SFQ) circuits and resonant tunnel devices, high-speed operation at the logic circuit level has not been proven for these new technologies and they have many unknowns. SFQ circuits, for which integrated circuit operation on the scale of 10,000 junctions has already been proven, can be called the most promising candidate for post-CMOS technology.

Table 1 New logic device technologies and their performance (Source: ITRS roadmap)

	Dimensions	Circuit Speed	Operation Energy
SFQ devices	300 nm	250–800 GHz	2×10^{-19} J
One-dimensional FET devices	100 nm	30 GHz	2×10^{-18} J
Resonant tunnel devices	100 nm	30 GHz	$> 2 \times 10^{-18}$ J
Single-electron devices	40nm	1 GHz	1×10^{-18} J
Molecular devices	unknown	1 MHz	1×10^{-16} J
Quantum cell automatons	60 nm	1 MHz	1×10^{-18} J
Spin devices	100 nm	30 GHz	2×10^{-18} J

SFQ circuits are logic circuits that use single-flux quantum, a minute physical quantity, as an information carrier, and they operate at extremely high speed with low power consumption. Their operating speed improves in proportion to the dimensions of their Josephson junctions, but the maximum value is ultimately limited by the superconducting energy gap. Table 2 shows the performance limit on SFQ circuits when Nb is used. A clock frequency some 10 times better than the performance limit of 22 nm CMOS (16 GHz, 3G transitors/cm^2) can be expected with SFQ circuits. The low integration density can be compensated by three-dimensional integration. In addition, by using oxide-based superconducting materials, clock frequencies reaching tera hertz are possible. Furthermore, with SFQ circuits, light-speed ballistic conduction of the SFQ pulses that make use of superconducting transmission lines is possible, as is inter-gate

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communication that is not limited by wiring delay. That is why SFQ circuits can build high-performance information processing systems that would be impossible to create with CMOS circuits.

Table 2 Limit of SFQ circuit performance
(When Nb material is used. Large-scale system, such as a microprocessor, is envisioned.)

Junction size	0.3 μm
Critical current density	100 kA/cm^2
Clock frequency	125 GHz–250 GHz
Power consumption	25 nW/gate–50 nW/gate
Integration density	Up to 100 M junctions/cm^2

Currently, development of SFQ microprocessors is underway at Nagoya University and Yokohama National University with an eye on realizing the high-performance servers of the future. Figure 1 shows the progress that has been made in SFQ microprocessor performance. Since the microprocessor that has been developed has few commands and a shorter word length than CMOS, a direct comparison with CMOS would be impossible, but the latest design achieves 1 GOPS compared with a CMOS microprocessor, and performance evaluations by means of tests are now underway. With the use of miniaturization and multilayering, proven performance exceeding CMOS is just around the corner.

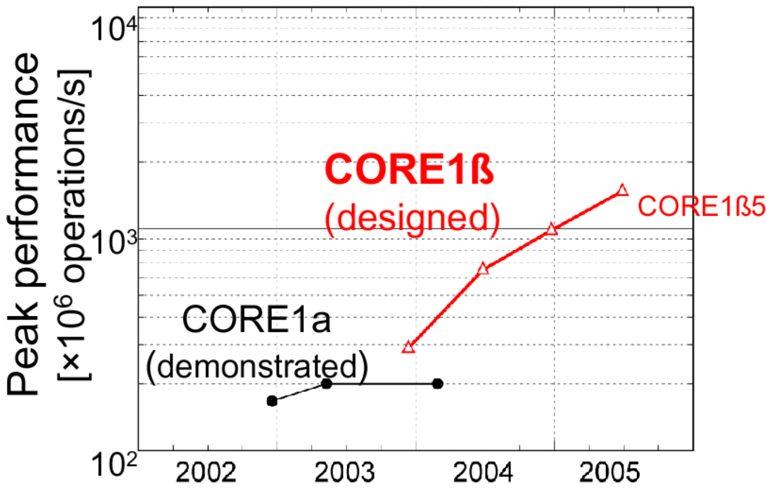

Fig. 1 Improving the performance of SFQ microprocessors. Operation has been proven for CORE1α. Design of CORE1β has been complete, and testing of operation performance is underway.

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Feature Articles: Advances in Superconducting Power/Industrial Equipment - SMES Deployment -

Shigeo Nagaya
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Electric Power Research and Development Center
Chubu Electric Power Co., Ltd.

Since superconducting technology in the field of electric power is characterized by the ability to efficiently handle large currents, it has wide-ranging upstream to downstream applications, including power generation, power transmission/transforming, and storage. It is expected to be one of the technologies underpinning electric power in the future, thanks to is broad applicability, high efficiency, and ability to conserve energy.

In addition, attention is being focused on the application of superconducting technology to issues relating to the quality of power that comes with price competition, and the introduction of distributed power sources in recent years, and there are high hopes for the practical use of superconducting magnetic energy storage (SMES).

SMES stows electric power as a magnetic field in a superconducting coil, and it is characterized by the ability to instantaneously release the power it is storing, the ability of the storage section to be freely configured by only the amount of energy necessary, and superconducting coils (the storage section and heart of SMES) that can handle repeated charging.

Based on its ability to instantaneously release a vast amount of power, the application of SMES to the field of electric power is being studied for stabilizing power networks and performing load compensation for voltage transforming in steel making and railways, which have a lot of repeated charging. However, progress is also being made toward its introduction into instantaneous voltage drop compensators, thanks to its ability to freely configure the storage section based only on the required amount of energy.

An instantaneous voltage drop is a phenomenon in which voltage lowers for about a second due to a lightning strike on a transmission line or some other cause. At the semiconductor and LCD plants with the latest equipment, such drops in voltage impacts plant operations and causes major damage.

One means of preventing this is to install an uninterruptible power supply (UPS) that uses batteries or another power source. A UPS will provide backup power during the voltage drop, but since instantaneous power drops are for the most part about 0.3 second long, the UPS must output a massive amount of power. The total amount of energy in order to compensate for the drop in voltage is output multiplied by time, which means adequate performance can be delivered up to about several kilowatt hours.

SMES displays characteristics exactly in this regard, as opposed to other power storage devices, and it is able to instantaneously release stored energy and store only the amount of energy need for the operating time. Among the various power storage technologies out there, double layer capacitors also exhibit such characteristics, but since they are capacitors, they have limits in terms of output, so when talking about

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output between several thousand kVA and 10,000 kVA, as is required by large scale plants, SMES is the optimal system in terms of specifications and performance.

At present, we are just beginning to test a 10,000 kVA system at Sharp Corporation's Kameyama Plant, following an actual field test there on SMES for compensating an instantaneous power drop of 5,000 kVA. SMES has performed beyond our expectations for instantaneous power drops that have occurred thus far, and its outlook from a technical standpoint is good.

The practical application of superconducting technologies and equipment in addition to SMES obviously requires that their costs, in respect to their functionality and capacity, be deemed appropriate from the user's perspective, or in other words, the switch to superconducting must be profitable. In that respect, reducing the cost is believed to key to the practical application of superconducting technologies.

In addition, the reliability of superconducting equipment in the latest SMES demonstration test was actually in the cooling technology for superconducting, rather than the superconducting section itself. When superconducting technology is introduced in electric power and other infrastructures, the reliability of this cooling technology will be decisive.

Under the present circumstances, the cooling technology is an issue, and maintenance beyond what was imagined is required. However, innovative technical development for the reliability of this cooling technology is underway in the national project for SMES development, and when the project ends in 2007, epoch-making cooling technology will be in ours.

We hope that such reliability will be secured that we can reach a level where users are not even aware that superconducting is in use, and we would like to aim for practical applications at the earliest possible time.

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Feature Articles: Advances in Superconducting Power/Industrial Equipment - Development of Superconducting Power Cables -

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Sumitomo Electric Industries, Ltd.

1. Advances in mass production and increased performance of high-temperature superconducting wire

The application of pressurized sintering has increased yields of bismuth-based high-temperature superconducting wire and improved its mechanical and electrical characteristics by a factor of 1.5. This enables the mass production of 1,600-m-long wires and critical current at 77 K of between 150 and 170 A (4-mm width). The applicability is widening to 200,000 Am at Ic x L (critical current x length) and to 500,000 Am at 1-cm width conversion. This is an improvement of even physical characteristics, such as Birr (irreversibility field) and Young's modulus, over conventional bismuth-based high-temperature superconducting wire, resulting in the emergence of a very different kind of superconducting wire.

Results of technological developments exceeding 100 m and 100 A (1-cm width), even with thin-film wire materials using YBCO and HoBCO, have been announced by five organizations worldwide (Sumitomo Electric Industries, SRL, Fujikura, SP, and AMSC), and they are attempting the challenge of commercializing such thin-film wire material.

2. Features and current state of high-temperature superconducting cables

There are increasing hopes for superconducting cables that will enable the transport of vast amounts of electric power with less energy and space by lowering cooling costs through the use of liquid nitrogen (77 K) as a cryogen. Specifically, according to the Energy Policy Act of 2005—established in August 2005 in the U.S., where the modernization of power networks has become a national issue—high-temperature superconducting cables are expected to be the trump card for solving power network problems.

High-temperature superconducting cables enable a capacity increase of two or three times by replacing existing cables when raising capacity on existing underground infrastructure, and even on newly build lines, distances are shorter and infrastructure lighter compared with overhead transmission lines, and environmentally friendly lines that are EMI-free, cost less, and conserve energy can be built. Since high-current transmission lines result, they have lower voltages than conventional lines and infrastructure is lighter, making it possible to inexpensively build transmission lines about which residents need not worry. Another feature of superconducting cables are their potential as new solutions to the increasing electric energy of the future, including the lowering of construction costs and conversion of high-voltage substations to low-voltage substations and low-voltage switching stations, through the conversion of conventional high-voltage transmission networks to super-conducting (low voltage) transmission networks. The use of liquid nitrogen as a cryogen also provides protection against explosions and fire, and delivers temperature uniformity (low heat cycle).

In addition, DC superconducting cables are an area in which major technical advances are expected.

With present technology, DC power transmission exceeding 10,000 A is possible, and this enables the transmission of the same amount of power with a required cross section only several tenths that of copper AC cable. This reduces transmission loss to about one-eightieth. Hopes are high for such things as interconnections with high-capacity distributed power sources (for example, solar power generation and wind power generation) as well as applications to DC power supply to Internet data centers where power loads concentrate, high capacity trunk lines, and interconnected power system lines.

Verification tests on the practicality of the 3-in-one 100 m, 114 MVA superconducting cable by Tokyo Electric Power Company (TEPCO), Sumitomo Electric Industries, and the Central Research Institute of Electric Power Industry (CRIEPI) were successfully concluded in 2002, and demonstrations of high-temperature superconducting cables are planned, first in the U.S., Europe, and Japan, and later in South Korea, China, and Mexico. In the U.S., demonstrations are underway simultaneously in three locations (Albany and Long Island in New York, and Columbus in Ohio) under the auspices of the State of New York and the Department of Energy. Table 1 provides an overview of the various projects.

The results of these projects are expected in 2007, and new developments toward the next step are anticipated.

Table 1 High-Temperature Superconducting Cable Projects

Project Name	Members	Utility	Sponsor	Budget	Line Condition	Insulation	Phase Config-uration	Material Used	Material Source	Test Period	Notes
TEPCO	Sumitomo Electric Industries	TEPCO		¥2 billion (US$18 M)	AC66kV–1000A–100m	low temperature	3-in-1	Bi2223	Sumitomo Electric Industries	2001–2002	
Copenhagen	NKT		Danish Energy Authority		AC30kV–2000A–30m	normal temperature	1x3	Bi2223	NST	2001–2003	
Southwire	Southwire		DOE		AC12.5kV–1250A–30m	low temperature	1x3	Bi2223	IGC	2000–	ongoing
Detroit	Pirelli	Detroit Edison	DOE		AC24kV–2400A–120m	normal temperature	1x3	Bi2223	AMSC	10.2001–	failed
Super-ACE	Super-GM (Furukawa Electric, CRIEPI)		METI, NEDO		AC77kV–1000A–500m	low temperature	1x1	Bi2223	-	2004–2005	no heat cycle
Yunnan	Innopower, InnoST, Shanghai Cable Works	Yunnan Electric Power	Chinese Ministry of Science and Technology, City of Beijing, and Yunnan Province	35 million yuan (US$4.3 M)	AC35kV–2000A–33.5m	normal temperature	1x3	Bi2223	InnoST	4.2004–	
DAPAS	LG cable, KERI, KIMM	Korea Electric Power	[South] Korean Ministry of Science and Technology		AC22.9kV–1250A–75m	low temperature	3-in-1	Bi2223	AMSC	5–12.2004	
Lanzhou	Chinese Academy of Science, (Chang Tong Cable Co.)				AC10.5kV–1500A–75m	normal temperature	1x3	Bi2223	AMSC	2005–	
KEPRI	KEPRI, Sumitomo Electric Industries, KERI, KBSI and other universities	Korea Electric Power	South Korean government	¥240 million	AC22.9kV–1250A–100m	low temperature	3-in-1	Bi2223	Sumitomo Electric Industries	2005–	
Albany	SuperPower, Sumitomo Electric Industries, BOC	Niagara Mohawk	DOE, NYSERDA	US$26 million	AC34.5kV–800A–350m	low temperature	3-in-1	Bi2223 (YBCO*)	Sumitomo Electric Industries (SP*)	2005–	* replaced with 30-m YBCO cable on latter half
LIPA	AMSC, Nexans, Air Liquide	Long Island Power Authority	DOE	US$30 million	AC138kV 2400A–660m	low temperature	1x3	Bi2223	AMSC	2006–	
Ohio	Ultera, ORNL	American Electric Power	DOE	US$9 million	AC13.2kV 3000A–200m	low temperature	3-phase coax	Bi2223	AMSC	2006–	

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Feature Articles: Advances in Superconducting Power/Industrial Equipment
- Development Status of Superconducting Fault Current Limiters (SFCL) -

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In the Research and Development of Fundamental Technologies for a Superconducting AC Power Equipment project, we developed S/N transition-type SFCLs that used YBCO thin films and a reactor for a rectifier-type SFCL that uses Bi-2223 wire. Mitsubishi Electric and Toshiba were in charge of the S/N transition-type SFCLs. Mitsubishi Electric developed a 1 kA-class SFCL for the development of large-current technologies, while Toshiba developed a 6.6 kV SFCL for the development of high-voltage technologies.

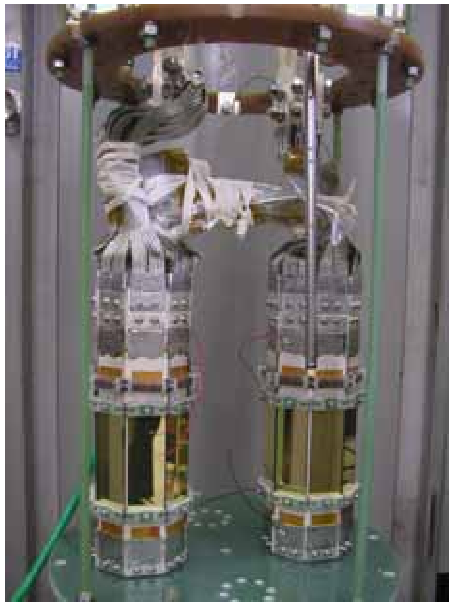

Fig. 1 Photo of 1 kA-class SFCL element

Mitsubishi Electric developed a structure that aimed to uniformly distribute current and reduce AC loss by connecting in parallel and in an octagonal arrangement eight pieces of 3 x 10 cm YBCO thin film on which gold had been deposited (see Figure 1). Two of these were connected in series, and one hour of continuous current was verified at 1 kA and five minutes at 1.2 kA, and it was also verified that fault current exceeding a peak value of 20 kA when there was no SFCL was limited to 5.22 kA.

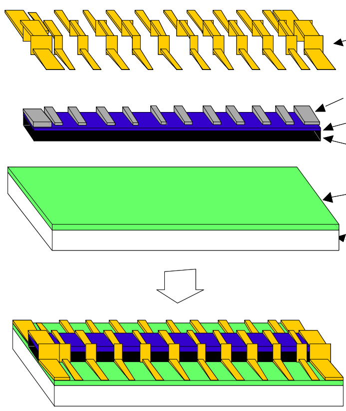

Fig. 2 Structure of high-voltage SFCL element

Toshiba developed a structure connecting 1 x 12 cm pieces of YBCO thin film at 1-cm intervals on Ni thin film via indium (see Figure 2). Forty of these elements were connected in series, and using a resonant power source, fault current limiting operation at a peak value of 10.9 kV and about 500 A was verified. Furthermore, the SFCL constructed with four elements series connection was introduced on to a model system assumed that the short-circuit capacity was increased caused by connecting distributed power supplies to a 6.6 kV distribution system, and it was verified that it could withstand operation on the model system in Power System Simulator in CRIEPI. Moreover, at High Power Testing Laboratory in CRIEPI, SFCLs connecting 20, 30, and 40 of the elements in series were used to verify that breakdown voltage per element did not drop due to increase in the number of elements connected in series. The maximum breakdown voltage in this case was about 14 kVrms with a module connecting 40 of the elements in series.

In addition, Toshiba developed a 66-kV 750-A pulse magnet (see Figure 3). Tests on its cooling characteristics and rated current were conducted. Worth particular mention are the withstand-voltage tests that were conducted using a 66-kV power apparatus conforming to JEC. Between the electrodes and ground, the test passed at AC 140 kVrms for one minute and at three lightning impulses of 350 kV at both polarities, while between the magnet electrodes, the test passed at three lightning impulses of 350 kV at both polarities. A fault current-limiting test that included in a rectifier circuit was also conducted.

Fig. 3 Superconducting coil housed in its casing

Overseas, SFCLs using Bi-2212 cylinders manufactured by NEXANS are being developed, and they are being applied to the CURL 10 project in Europe and the Matrix Fault Current Limiter project in the U.S.

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Feature Articles: Advances in Superconducting Power/Industrial Equipment - Current Status of Superconducting Transformers -

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Kyushu University

In our report of the current development status of superconducting transformers, we will reconfirm the significance of making transformers superconductive, and then based on this, explain the present state of development. The advantages of making transformers superconductive are generally considered to be their small size, light weight, and high efficiency compared with conventional equipment. Some naysayers complain that there is no reason to invest in developing further efficiency by superconductivity because existing equipment already exhibits power efficiency exceeding 99%, and small size and light weight are not much recognized as a product of increased efficiency. The basic parameter in transformer design is "one-turn voltage." Normally, the primary and secondary voltage of a transformer is determined by standards, and if we let B be the saturated magnetic flux of the core, S the cross section, and n the number of turns in the winding, then voltage V of both the primary and secondary will be given by $V = -d(nBS)/dt$. In this equation, B is nearly a constant $B = 1.5\text{-}1.7T$, but cross-section S and number of turns n can be freely set. Consequently, when switching to superconductivity, the core cross-section S can be decreased and the number of turns n increased compared with non-superconducting transformers. This corresponds to a drop in voltage per turn, and in the world of non-superconducting transformers, this is generally known as installation using the normal copper conductors. If we could achieve a low-loss state without increasing the physical size of the winding, even when the number of turns rises, by using the characteristic low loss and high current density of superconducting wire, not only would the core be thinner and lighter, but also the winding would be lighter and compact, enabling a small and lightweight transformer. The majority of heat load at low temperature is AC loss that occurs on the winding, and it can be said that the decision on making transformers superconducting depends on the reduction of loss in superconducting wire. The power required for cooling and the weight and dimensions of the cooling system are determined by the size of the AC loss. Important here is the fact that the majority of the power required for cooling converts into heat as a cooling penalty. The advantages of superconductivity, i.e. small size, light weight, and increased efficiency can be realized only after this heat falls below the Joule loss produced by the copper windings of conventional transformers. Ninety-nine percent efficiency means 1% of transmitted energy is converted to heat. If this could be reduced to one-fifth or one-forth by switching to superconductivity, the cooling system, too, could be reduced to one-fifth or one-forth. Heat release/cooling equipment accounts for half of the physical size of transformers, and in the case of underground substations in particular, it is not much known that the facilities/construction cost for cooling is about equal to or higher than the transformer itself. Even 1% heat release is an immense amount of transmission energy and difficult to cool. Ultimately, if the current loss of superconducting windings decreases, it will be possible to greatly reduce the one-turn voltage, create installations using normal copper conductors, and house the entire reduced-size core in a cryostat. In this case, the cryostat material can be inexpensive steel as in conventional models, instead of GFRP. This is the ultimate ideal form of a superconducting transformer.

Research and development is underway in pursuit of this ideal form of superconducting transformer, primarily in Japan, the U.S., and Europe, but also lately in South Korea and China. What follows is a report focused on the latest prototypes from the standpoint that the cutting edge of equipment research and development is testing that uses prototypes.

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In the U.S., Waukesha Electric Systems, SuperPower, Energy East, and the ORNL research group, with assistance from the Department of Energy (DOE), manufactured a three-phase, 24.9-kV/4.2-kV, 5/10-MVA transformer between 2003 and 2004 and is currently testing its characteristics with an eye on developing a 138-kV/13.8-kV, 30-MVA model. Just as in the previously described ideal transformer, the entire core is housed in a tank. The cooling system uses a cryocooler in which the natural convection of He gas cools the winding. The operating temperature is between 30 K and 77 K. However, since core loss is rather high at present, the core is thermally isolated from the winding by a liquid nitrogen shield, so that it operates nearly at room temperature. However, this first try ended in failure because dielectric breakdown occurred at voltages far lower than the rated voltage. This year and last, they removed the winding from the tank to try to find out why this was happening, but it is not difficult to imagine that the dielectric breakdown is being caused by the low dielectric strength of the He gas. They also came up with a conceptual design for a separate 30-MVA transformer, and came to the conclusion that Jc performance is inadequate and AC loss too high with current Bi-2223 wire. They have, therefore, announced that they will begin developing the transformer using Y-based wire.

Fig. 1 A 3ϕ 24.9-kV/4.2-kV, 5/10 MVA prototype transformer manufactured by WES. The transformer is housed in a steel tank.

In Japan, the Fukuoka Industry, Science & Technology Foundation (Fukuoka IST) manufactured a liquid-nitrogen-cooled, single-phase, 22-kV/6.9-kV, 1 MVA prototype transformer during a Regional Consortium Project commissioned by the New Energy and Industrial Technology Development Organization (NEDO), and in 2000, Kyushu Electric Power incorporated it into a subcooled liquid nitrogen circulation unit at its Imajuku substation and performed the first system interconnection test in Japan. The technical development of a spot-network-class superconducting transformer for electric power was concluded successfully. In the Super-ACE (Research and Development of Fundamental Technologies for Superconducting AC Power Equipment) project that followed this, Fuji Electric Systems Co., Ltd. manufactured a prototype single-phase 66-kV/6.9-kV, 2-MVA distribution transformer in 2003 and went as far as a factory

Fig. 2 A Fuji Electric Systems' prototype 1ϕ 66-kV/6.9-kV, 2 MVA transformer

test. The core is kept at room temperature, the winding is housed in a GFRP cryostat, and cooling is performed using a subcooled liquid nitrogen (66 K) circulation unit that combines a cryocooler and a pump. Except for a short-circuit test, this prototype soundly passes all other tests, including a 350-kV lightning impulse withstand voltage test and a 140-kV AC overvoltage test, as per JEC standards, and it was able to technically demonstrate the possibility of a nitrogen-cooled distribution-class transformer. However, efficiency at a cooling penalty of 10 is 99.5%, an improvement of 0.5% over conventional transformers, but realizing the previously mentioned ideal form of transformer requires that the AC loss of the wire be dramatically reduced.

In Japan, the Railway Technical Research Institute manufactured a prototype single-phase 25-kV/1.2-kV/0.4kV, 4 MVA transformer and is assessing its characteristics with an eye on reducing the weight of the transformers installed on bullet trains. The core is kept at room temperature, while for cooling, a subcooled liquid nitrogen system using natural convection is being employed by the cryostat. While current transformers weigh more than 3 tons, the prototype is only 1.7 tons when the cryostat is excluded. The design used in this case is an attempt to employ the high current density and low loss of superconducting wire by lowering the previously mentioned one-turn voltage below conventional transformers and enabling installation using the normal copper conductors. However, in order to ensure maintenance-free operation, incorporating a cryostat fit for the AC loss of 6 kW that occurs on the prototype results in its total weight far exceeding that of current transformers. In a bid to truly lighten transformers by reducing the AC loss of superconducting wire, the Railway Technical Research Institute this year launched a new four-year project with financial backing from the Ministry of Land, Infrastructure and Transport.

Fig. 3 A Railway Technical Research Institute prototype 1ϕ 25-kV/1.2-kV/0.4kV, 4 MVA transformer for bullet trains

In Europe, ABB manufactured a prototype three-phase 18.7-kV/0.42-kV, 630-kVA transformer and is carrying out a long-term system test, while Siemens manufactured a prototype 1-MVA transformer for railcar use. However, research and development on transformers is currently at a standstill in Europe.

The economic feasibility of switching to superconducting transformers is seen as being quite low as long as the focus is on verifying prototypes and a dramatic cut in the AC loss of the superconducting wire is not achieved, and this is not limited only to transformers. Even in Japan, there are new plans for the development of superconducting equipment that uses Y-based wire, and we expect that the pursuit of reduced AC loss will begin in earnest, combined with an improved Jc characteristic.

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Feature Articles: Advances in Superconducting Power/Industrial Equipment - Superconducting High-Gradient Magnetic Separation for Purification of Wastewater from Paper Factory -

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Shinichi Takeda, Assistant
Division of Sustainable Energy and Environmental Engineering
Graduate School of Engineering, Osaka University

Paper recycling is one of the crucial issues for building a recycling-oriented and sustainable society. We have developed a small-footprint system that uses a superconducting magnet to quickly and inexpensively carry out the advanced purification of the vast quantities of water used in processes at recycled-paper factories. The system we developed attaches small highly magnetic particles to suspended solids and organic components (for example, dyes, pigments, adhesives, and flocculants) or, conversely, makes these substances attach to the small highly magnetic particles, and then uses a high-gradient magnetic field generated by a superconducting magnet to perform highly efficient magnetic separation. At present, the system is processing 2,000 t/day at recycled-paper factories. The research and development on this system was a four-year project launched in 2001. The project was entitled Superconducting High-Gradient Magnetic Separation for Purification of Wastewater from Paper Factories and was carried out with support from NEDO's program for promoting research on fundamental technology (commissioned by Futaba Shoji Co., Ltd.).

A recycled-paper factory uses a massive amount of water (5,000 tons/day at a medium-sized factory) and outputs a similar amount of wastewater. Emission standards have been strengthened in recent years (COD < 20 ppm), and the costs of satisfying such standards are mounting, resulting in economic problems for factories. For example, introducing biological treatment equipment at a 5,000-ton-class factory necessitates an investment of several hundreds of millions of yen, and using sewers costs about ¥200 million a year. In either case, the cost of water purification is high, and a number for recycled-paper factories have actually ceased operations. That is why we got involved in developing a wastewater purification system that uses superconducting high gradient magnetic separation and can be introduced at recycled-paper factories. We have already completed a 2,000 ton/day system and introduced it at a factory where tests on its performance are underway.

Figure 1 shows photos and a conceptual diagram of the entire system. This system is installed on the later stage of ordinary equipment (pressure floatation unit) for the factory's wastewater. The wastewater treated by the pressure floatation unit is 200 ppm to several hundred ppm in COD and cannot be released as is. Our solution was to treat it using our superconducting high-gradient magnetic separation system, which purifies to a level at which the water can either be reused or released. As is shown in the figure, the factory's wastewater is first collected in a magnetic tank, and then wastewater containing flock (magnetic flock), to which highly magnetic particles are attached, is transferred from the magnetic tank to the settling tank. Magnetic separation of the magnetic flock is possible, but first the big, heavy flock that settles rapidly is separated to reduce the load on the magnetic filter installed within the superconducting magnet. The smaller and relatively lighter flock is then transferred from the settling tank along with the overflow to the magnetic separator, which is comprised of a superconducting magnet. Thin ferromagnetic wires (about 1 mm in diameter) are arranged within the superconducting magnet, and high-gradient magnetic field is formed in its vicinity. The magnetic flock is separated by being attracted to these wires (a magnetic filter) by the high-gradient magnetic field, and then the water can be reused as recycled water. The magnetic flock,

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separated by the lower part of the settling tank and the magnetic filter, is recovered as magnetic sludge, and a portion of this is reused as a magnetic agent (return sludge).

Results from a 200 ton/day test showed that purification up to a COD range of 38 ppm to 60 ppm was possible. With system optimization, the post-treatment COD value was lowered and a marked decrease in turbidity achieved, and we were able to confirm that the treated water could be reused.

The initial cost of this system is about ¥100 million. The cost of a 2,000 ton/day system using the conventional activated sludge method is several ¥100 million as previously mentioned. On the other hand, when discharging to the sewer, the annual cost becomes ¥200 million. Clearly, the initial cost of this system is considerably less than that of systems using the activated sludge method. A study of the system's running cost revealed that, including labor outlays, it costs about ¥130 per ton of water purified. On the other hand, the cost of using the sewer and purchasing new industrial water is ¥250 per ton. Based on this, we can say that the running cost of this system is about half that of the conventional method, and it therefore offers considerable economic advantages.

Overview of system we developed

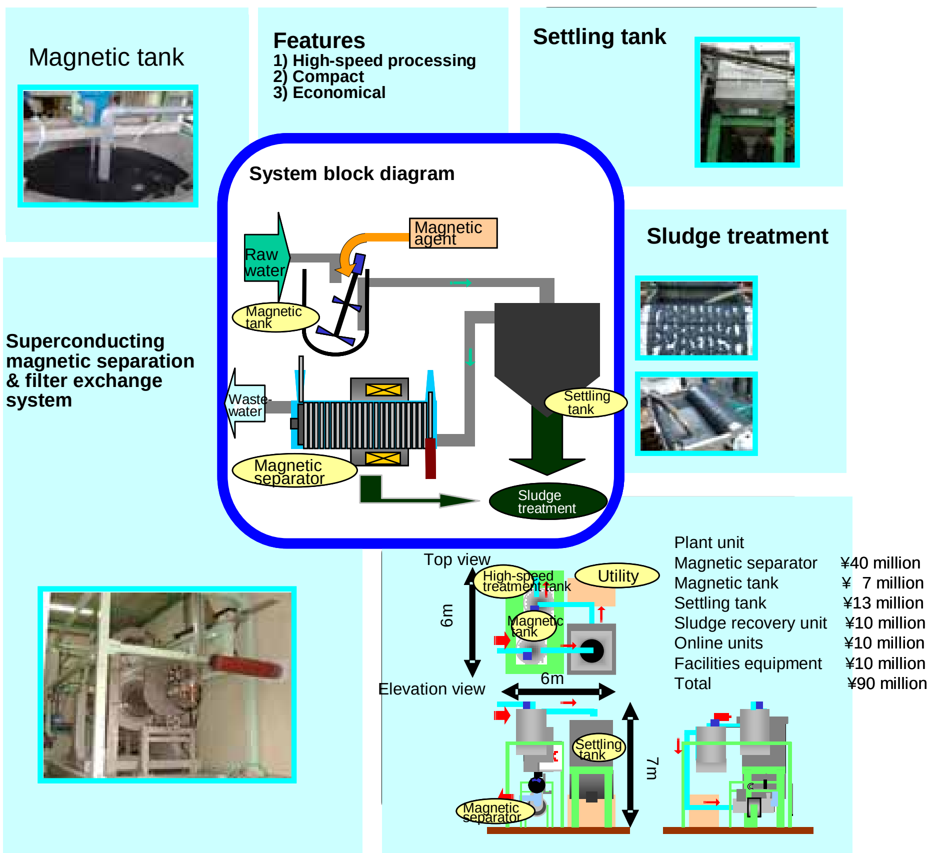

Fig. 1 Superconducting high-gradient magnetic separation system that we manufactured

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Patent Information

Introduction of Published Unexamined Patents in the First Half of Fiscal 2005

The following are ISTEC's patents published from April through September 2005. For more information, access the homepage of Japan Patent Office and visit the Industrial Property Digital Library (IPDL).

1) Publication No. 2005-252019: "Superconducting Electronic Devices"

Implementing single flux quantum (SFQ) circuits that operate at ultra-high speed requires that the top and bottom superconducting layers be separated by insulating interlayer with low dielectric constant and low dielectric loss. Conventionally, an insulating oxide for the insulating interlayer was selected with a view to ensuring superconducting characteristics in the superconducting layers, resulted in an oxide with high dielectric constant. That is why it has not been realized to fully bring out the high-speed potential of SFQ circuits. This patent achieved an insulating interlayer with low dielectric constant and low dielectric loss as well as high electrical insulating properties by employing a multilayered insulating film composed primarily of low-dielectric-constant MgO, without degrading the characteristics of the superconducting film. This reduces the parasitic capacitance of Josephson junctions and superconducting wiring, enabling the prevention of waveform distortion in high-frequency signals and making circuit design easier.

2) Publication No. 2005-252400: "Gate Blocks, Logic Circuits using them, and their Design Method"

This invention relates to the method of configuring signal lines that include the clock signal between logic gate blocks, and makes it easier to design single flux quantum (SFQ) circuits that operate at ultra-high speed. With the conventional method, a signal line was branched into plural lines outside gate blocks, but in this invention, the branching of a signal line is included in the design of a gate block configuration with considering the connection to the next gate blocks, and signal connections between gate blocks are made using only passive transmission lines. This invention remarkably reduces the number of receiver gates and driver gates for signal connection, thereby not only improving the integration density, but also improving operation speed and lowering power consumption.

3) Publication No. 2005-259812: "Superconducting SFQ Circuits"

This invention provides a superconducting single flux quantum (SFQ) integrated circuit in which a partial ground-potential fluctuation of some circuit block in the SFQ integrated circuit does not malfunction other circuit blocks in the SFQ integrated circuit. The SFQ integrated circuit in this invention has plural grounding electrodes. The integrated circuit is comprised of SFQ circuit bullock No.1 connected to grounding electrode No. 1, SFQ circuit block No.2 connected to grounding electrode No.2, and a separating superconducting SFQ circuit block that connects SFQ circuit blocks No.1 and No. 2. Furthermore, it is characterized by a connection between grounding electrode No. 1 and No. 2 by means of inductive wiring.

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4) Publication No. 2005-260364: "Superconducting Latching Driver Circuits"

This invention provides superconducting latching driver circuits that are applied with DC bias current and are designed to generate adequate output voltage. Conventionally, AC bias current was applied to Josephson junctions to reset latching driver circuits, but this bias current brought about fluctuations in grounding potential, which severely limited the operating margin. To latch onto SFQ pulses, superconducting latching driver circuits from this invention contain a latching circuit comprising Josephson junctions with hysteresis characteristics, a load circuit comprising load inductance and load resistance connected to the output of the latching circuit, as well as a reset circuit between the output of the latching circuit and the load circuit, and they are characterized by the biasing of the Josephson junctions in the latching circuit with DC current. Once the latching circuit latches onto SFQ pulses, the reset circuit will reset it after a predetermined time.

(Katsuo Nakazato, Director, Research & Development Promotion Division, SRL/ISTEC)

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Standardization Activities

Topics in September

- IEC/TC90 to Hold Ad Hoc Group Conferences in U.S. and EU -

The IEC/TC90 will be holding ad hoc group meetings regarding "uncertainty" and "superconducting current leads" in the U.S. and Europe between August and September 2005.

—Ad hoc group 2 conference—
• Rapporteur: Loren F. Goodrich (U.S.)
• Date: August 29, 2005 (during the CEC/ICMC 2005: Cryogenic Engineering Conference and International Cryogenic Materials Conference [CEC/ICMC 2005] session)
• Location: Keystone, CO, U.S.
• Topic: Dealing with "Uncertainty" in Superconducting Standards

—Ad hoc group 1 conference—
• Rapporteur: Kozo Osamura (Kyoto University)
• Date: September 14, 2005 (during the 7th European Conference on Applied Superconductivity [EUCAS'05] session)
• Location: Vienna, Austria
• Topic: International Standardization of "Designs for Superconducting Current Leads and General Requirements for Characteristic Tests"

—Ad hoc group 1 conference—
• Rapporteur: Kozo Osamura (Kyoto University)
• Date: September 21, 2005 (during the 19th International Conference on Magnet Technology [MT-19] session)
• Location: Genoa, Italy
• Topic: Continued Discussion of International Standardization of "Designs for Superconducting Current Leads and General Requirements for Characteristic Tests"

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Topics in November

- Second and Third Ad Hoc Group 1 (Current Leads) Conferences to Be Held -

Ad hoc group 1 of the IEC/TC90 (superconductivity) held the second and third ad hoc group conferences (Rapporteur: Kozo Osamura, Kyoto University) on September 15 and 21, 2005 in Vienna and Genoa, respectively. The conferences were held jointly with EUCAS'05 and MT-19, respectively. The first conference had been held in October 2004 in Florida, U.S.

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Kozo Osamura (Professor, Kyoto University), Takakazu Shintomi (Professor, Nihon University), and Ken-ichi Sato (Secretary, Sumitomo Electric Industries) were sent to the conferences from Japan (JNC). The local attendees were as follows:

—Vienna conference (second): T. Arendt (EAS), A. Ballarino (CERN), T. Taylor (CERN), J. Sosnowski (Poland), T. Shintomi (Nihon University), K. Sato (Sumitomo Electric Industries), and K. Osamura (Kyoto University)

—Genoa conference (third): R. Heller (FzK), W. Fietz (FzK), H. Krauth (EAS), T. Taylor (CERN), T. Mito (National Institute for Fusion Science), T. Shintomi (Nihon University), K. Sato (Sumitomo Electric Industries), K. Osamura (Kyoto University)

The purpose of ad hoc group 1 is to have international specialists debate the necessity for international standards of current leads, which are essential to superconducting equipment, and to report the results of its activities and the direction of standardization at the IEC/TC90 international conferences.

An overview of the conferences is provided below.

(1) An international consensus was reached on the necessity for international standardization of current leads, which are essential to superconducting equipment.
(2) Discussion was continued on the comments put forth by EU and U.S. members about the draft (ver. 7) presented by the JNC.
(3) The title will be general current leads, and not be limited to superconducting current leads.
(4) The publishing of patent policy items will be deferred.
(5) The organization standards content will eliminate design items, explain the concept (principle) of current leads, and add a description of the essential characteristics for configuring current leads and a characteristic test for them.
(6) Heat load, mass flow, pressure drop, voltage drop, high voltage measurements, safety margin in case of loss of mass flow, and leak tightness—essential items for current leads—were mentioned as characteristic items essential to current leads.
(7) It was pointed out that a concrete elaboration would be better left until after the establishment of a working group (WG).

Next, the ad-hoc group 1 conference will sum up the intentions of EU and U.S. members and then determine the appropriate direction to be taken after reaching agreement with ad hoc group 1 members.

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(Yasuzo Tanaka, Director, Standardization Department, ISTEC)

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